

Pin Definition:

1. Source 1	8. Drain 1
2. Gate 1	7. Drain 1
3. Source 2	6. Drain 2
4. Gate 2	5. Drain 2

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (m Ω)	I_D (A)
-30	60 @ $V_{GS} = 10V$	-4.9
	90 @ $V_{GS} = 4.5V$	-3.7

Features

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

Application

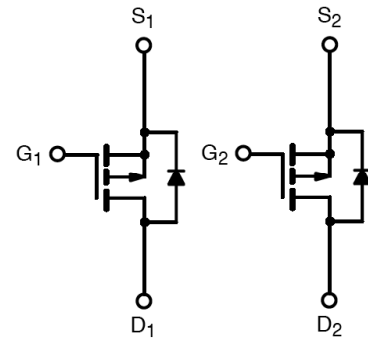
- Load Switch
- PA Switch

Ordering Information

Part No.	Package	Packing
TSM4953DCS RLG	SOP-8	2.5Kpcs / 13" Reel

Note: "G" denotes Halogen Free Product.

Block Diagram



Dual P-Channel MOSFET

Absolute Maximum Rating ($T_a = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current, $V_{GS} @ 4.5V$.	I_D	-4.9	A
Pulsed Drain Current, $V_{GS} @ 4.5V$	I_{DM}	-20	A
Continuous Source Current (Diode Conduction) ^{a,b}	I_S	-2.6	A
Maximum Power Dissipation	P_D	$T_a = 25^\circ C$	2.5
		$T_a = 70^\circ C$	1.3
Operating Junction Temperature	T_J	+150	$^\circ C$
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150	$^\circ C$

Thermal Performance

Parameter	Symbol	Limit	Unit
Junction to Case Thermal Resistance	$R_{\theta_{JC}}$	40	$^\circ C/W$
Junction to Ambient Thermal Resistance (PCB mounted)	$R_{\theta_{JA}}$	62.5	$^\circ C/W$

Notes:

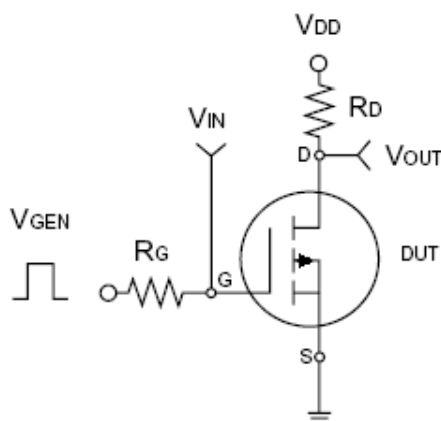
- Pulse width limited by the Maximum junction temperature
- Surface Mounted on FR4 Board, $t \leq 5$ sec.

Electrical Specifications (Ta = 25°C unless otherwise noted)

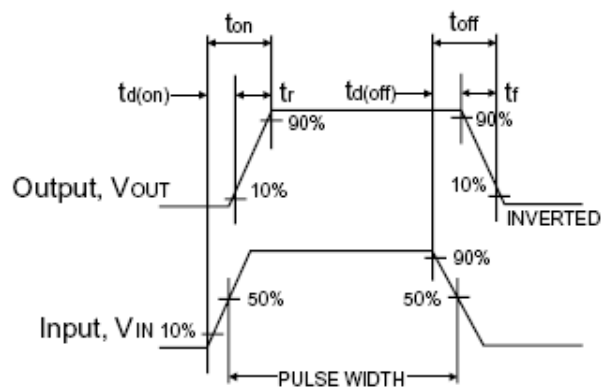
Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = -250\mu A$	BV_{DSS}	-30	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu A$	$V_{GS(TH)}$	-1.0	-1.5	-3.0	V
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
Zero Gate Voltage Drain Current	$V_{DS} = -24V, V_{GS} = 0V$	I_{DSS}	--	--	-1.0	μA
On-State Drain Current ^a	$V_{DS} = -5V, V_{GS} = -10V$	$I_{D(ON)}$	-6	--	--	A
Drain-Source On-State Resistance ^a	$V_{GS} = -10V, I_D = -4.9A$	$R_{DS(ON)}$	--	50	60	m Ω
	$V_{GS} = -4.5V, I_D = -3.7A$		--	75	90	
Forward Transconductance ^a	$V_{DS} = -15V, I_D = -4.9A$	g_{fs}	--	10	--	S
Diode Forward Voltage	$I_S = -1.9A, V_{GS} = 0V$	V_{SD}	--	--	-1.3	V
Dynamic						
Total Gate Charge	$V_{DS} = -15V, I_D = -4.9A,$ $V_{GS} = -10V$	Q_g	--	28	--	nC
Gate-Source Charge		Q_{gs}	--	3	--	
Gate-Drain Charge		Q_{gd}	--	7	--	
Input Capacitance	$V_{DS} = -15V, V_{GS} = 0V,$ $f = 1.0MHz$	C_{iss}	--	745	--	pF
Output Capacitance		C_{oss}	--	440	--	
Reverse Transfer Capacitance		C_{rss}	--	120	--	
Switching						
Turn-On Delay Time	$V_{DD} = -15V, R_L = 15\Omega,$ $I_D = -1A, V_{GEN} = -10V,$ $R_G = 6\Omega$	$t_{d(on)}$	--	9	--	nS
Turn-On Rise Time		t_r	--	15	--	
Turn-Off Delay Time		$t_{d(off)}$	--	75	--	
Turn-Off Fall Time		t_f	--	40	--	

Notes:

1. pulse test: $PW \leq 300\mu S$, duty cycle $\leq 2\%$
2. For DESIGN AID ONLY, not subject to production testing.
3. Switching time is essentially independent of operating temperature.



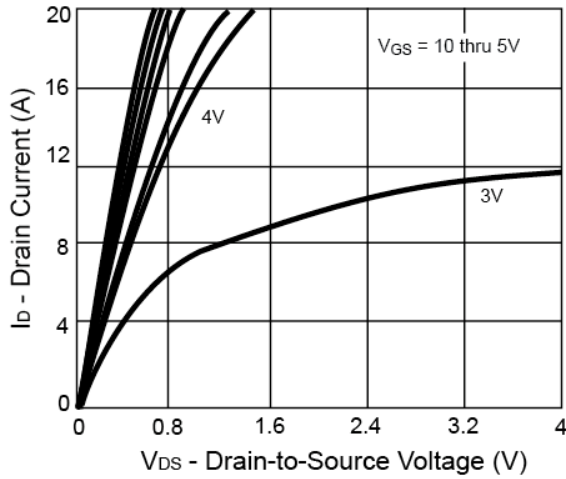
Switching Test Circuit



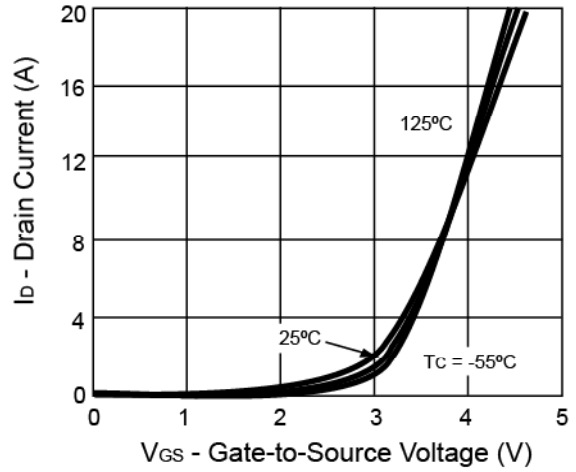
Switchin Waveforms

Electrical Characteristics Curve ($T_a = 25^\circ\text{C}$, unless otherwise noted)

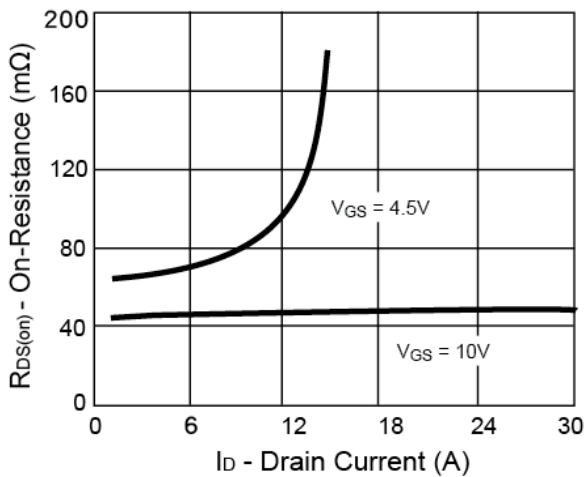
Output Characteristics



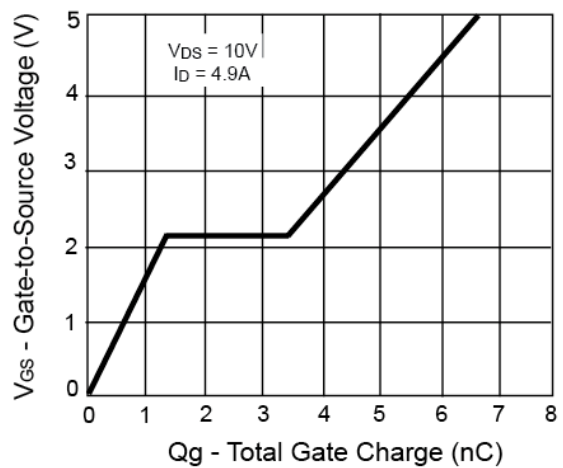
Transfer Characteristics



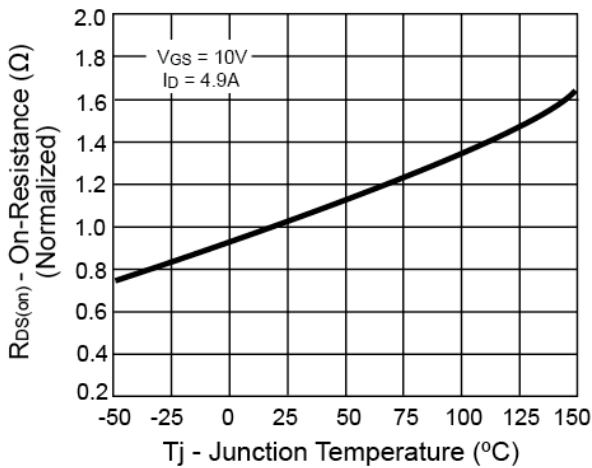
On-Resistance vs. Drain Current



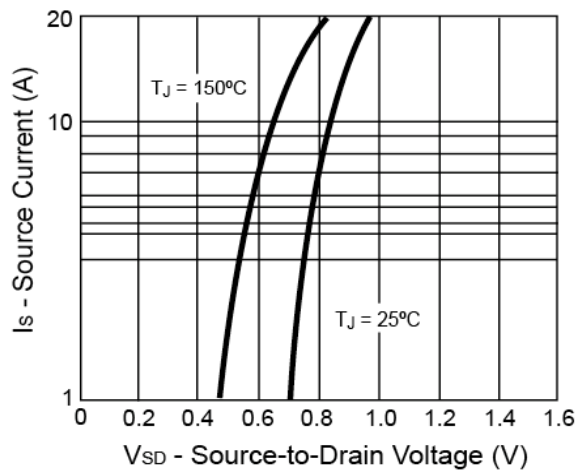
Gate Charge



On-Resistance vs. Junction Temperature

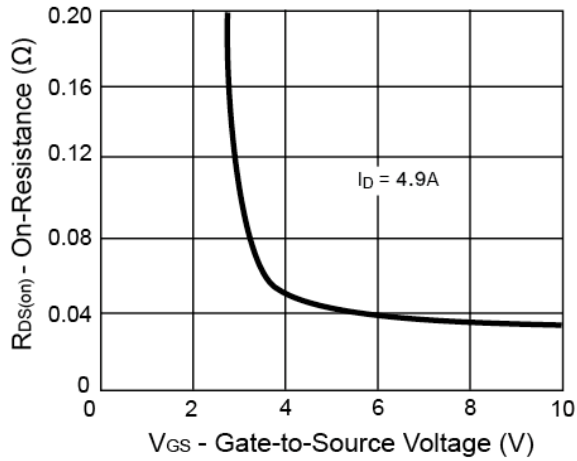


Source-Drain Diode Forward Voltage

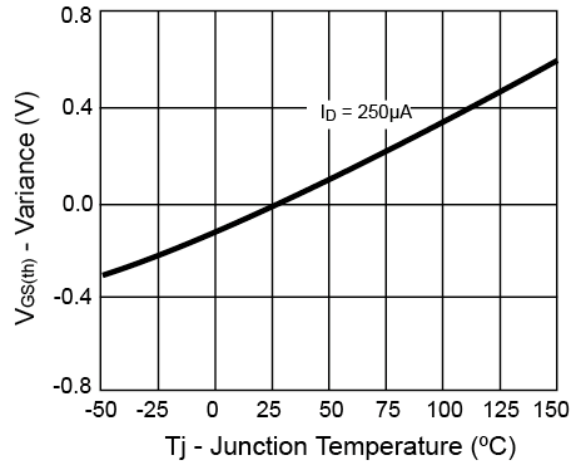


Electrical Characteristics Curve ($T_a = 25^\circ\text{C}$, unless otherwise noted)

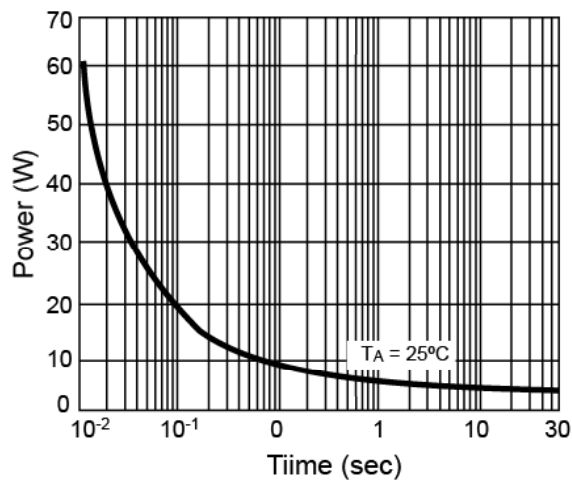
On-Resistance vs. Gate-Source Voltage



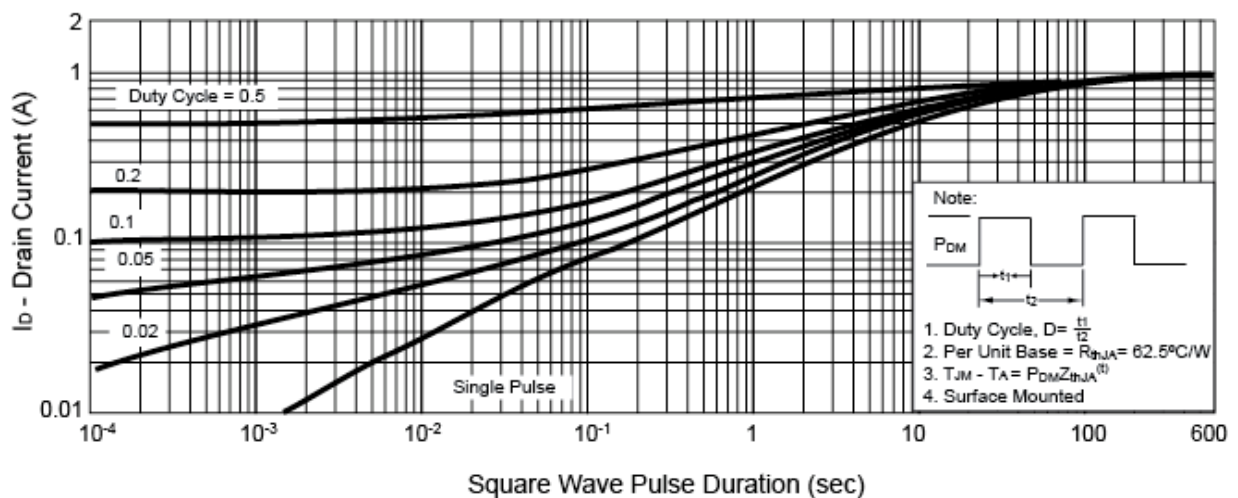
Threshold Voltage



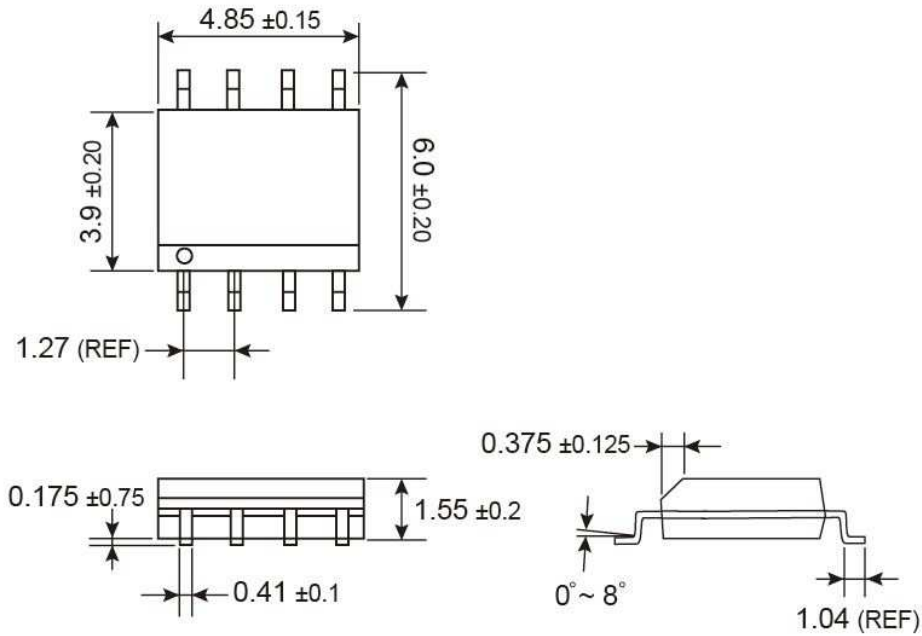
Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient

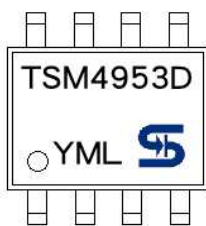


SOP-8 Mechanical Drawing



Unit: Millimeters

Marking Diagram



- Y = Year Code
- M = Month Code for Halogen Free Product
 - O =Jan P =Feb Q =Mar R =Apr
 - S =May T =Jun U =Jul V =Aug
 - W =Sep X =Oct Y =Nov Z =Dec
- L = Lot Code

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