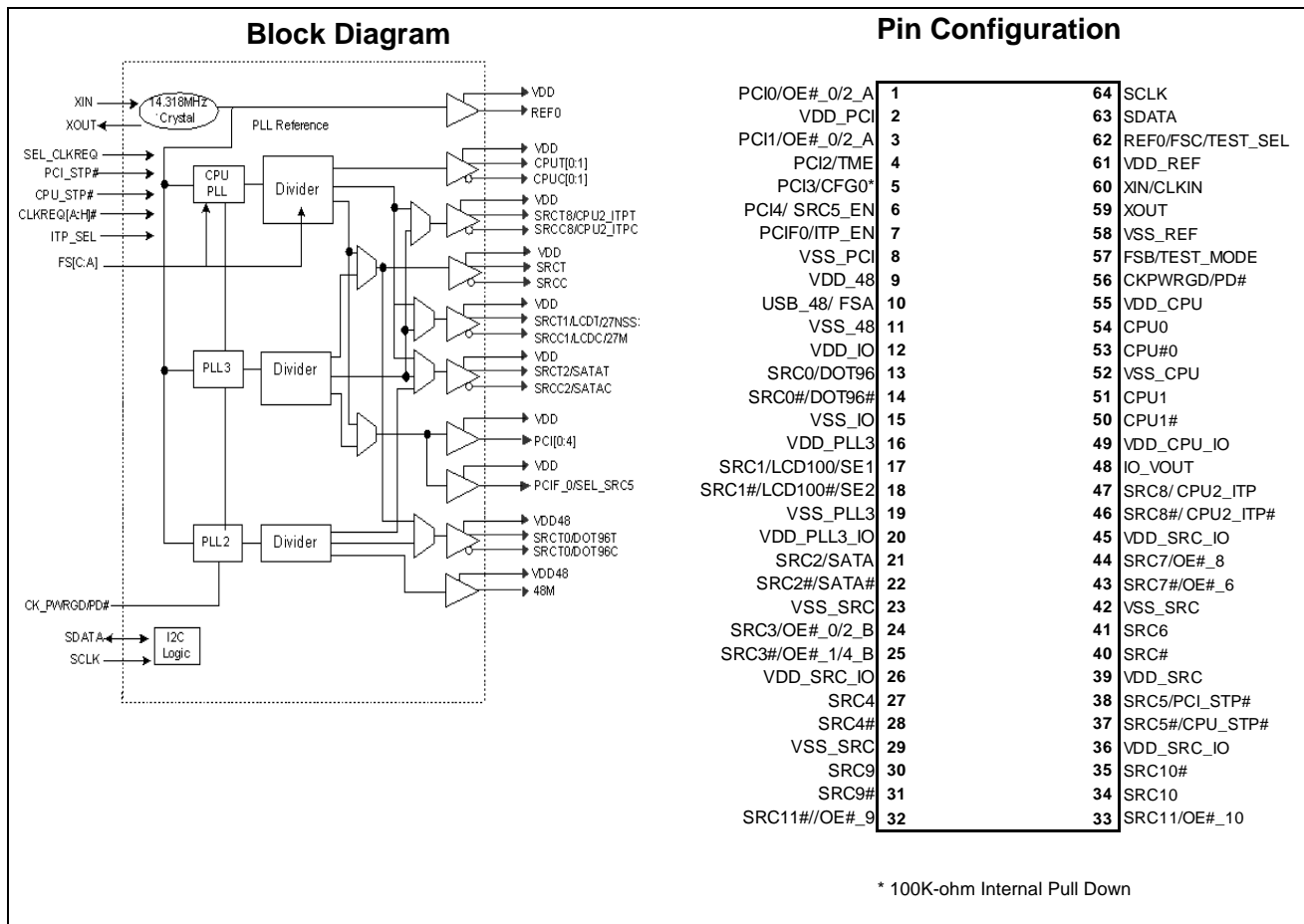# SILICON LABS

SL28506

Clock Generator for Intel® Eaglelake Chipset

Features

- Intel® CK505 Rev. 1.0 Compliant
- Low power push-pull type differential output buffers
- PCI-Express Gen 2 Compliant SRC clocks (exclude SRC0 and SRC1)
- 8-step programmable drive strength for single-ended clocks
- Differential CPU clocks with selectable frequency
- 100 MHz Differential SRC clocks
- 100 MHz Differential LCD clock
- 96 MHz Differential DOT clock
- 48 MHz USB clock
- 33 MHz PCI clocks
- 27MHz non-spread Video clock
- 25 MHz Video clocks
- 1396 Firewire clock
- Buffered Reference Clock 14.318 MHz
- 14.318 MHz Crystal Input or Clock Input
- Low-voltage frequency select input
- I²C support with readback capabilities
- Ideal Lexmark Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction
- Industrial Temperature -40°C to 85°C
- 3.3V Power supply
- 64-pinTSSOP packages

CPU	SRC	PCI	REF	DOT96	USB_48	LCD	SE
x2 / x3	x7/12	x6	x 1	x 1	x 1	x1	x2

Block Diagram

Pin Configuration

PCI0/OE#_0/2_A	1	64	SCLK
VDD_PCI	2	63	SDATA
PCI1/OE#_0/2_A	3	62	REF0/FSC/TEST_SEL
PCI2/TME	4	61	VDD_REF
PCI3/CFG0*	5	60	XIN/CLKIN
PCI4/ SRC5_EN	6	59	XOUT
PCIF0/ITP_EN	7	58	VSS_REF
VSS_PCI	8	57	FSB/TEST_MODE
VDD_48	9	56	CKPWRGD/PD#
USB_48/ FSA	10	55	VDD_CPU
VSS_48	11	54	CPU0
VDD_IO	12	53	CPU#0
SRC0/DOT96	13	52	VSS_CPU
SRC0#/DOT96#	14	51	CPU1
VSS_IO	15	50	CPU1#
VDD_PLL3	16	49	VDD_CPU_IO
SRC1/LCD100/SE1	17	48	IO_VOUT
SRC1#/LCD100#/SE2	18	47	SRC8/ CPU2_ITP
VSS_PLL3	19	46	SRC8#/ CPU2_ITP#
VDD_PLL3_IO	20	45	VDD_SRC_IO
SRC2/SATA	21	44	SRC7/OE#_8
SRC2#/SATA#	22	43	SRC7#/OE#_6
VSS_SRC	23	42	VSS_SRC
SRC3/OE#_0/2_B	24	41	SRC6
SRC3#/OE#_1/4_B	25	40	SRC#
VDD_SRC_IO	26	39	VDD_SRC
SRC4	27	38	SRC5/PCI_STP#
SRC4#	28	37	SRC5#/CPU_STP#
VSS_SRC	29	36	VDD_SRC_IO
SRC9	30	35	SRC10#
SRC9#	31	34	SRC10
SRC11#//OE#_9	32	33	SRC11/OE#_10

* 100K-ohm Internal Pull Down

400 West Cesar Chavez, Austin, TX 78701   1+(512) 416-8500   1+(512) 416-9669   www.silabs.com

64 TSSOP Pin Definition

Pin No.	Name	Type	Description
1	PCI0/OE#_0/2_A	I/O, SE	3.3V, 33MHz clock/3.3V OE# Input mappable via I2C to control either SRC0 or SRC2. *(Default PCI0, 33MHz clock)*
2	VDD_PCI	PWR	3.3V Power supply for PCI PLL.
3	PCI1/OE#_1/4_A	I/O, SE	3.3V, 33MHz clock/3.3V OE# Input mappable via I2C to control either SRC1 or SRC4. *(Default PCI1, 33MHz clock)*
4	PCI2/TME	I/O, SE	3.3V tolerance input for overclocking enable pin/3.3V, 33MHz clock. *(Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications)*
5	PCI3/CFG0	I/O, SE, PD	3.3V tolerant input for CPU frequency selection/3.3V 33MHz clock. *(Refer to DC Electrical Specifications table for Vil_PCI3/CFG0 and Vih_PCI3/CFG0 specifications).*

CFG [1:0]	PCI2/TME	PCI3/CGF0	Mode	PLL1		PLL2		PLL3	
				Output	SSC	Output	SSC	Output	SSC
00	x	Low	0 -Def	CPU / SRC / PCI33	Down	USB	NA	--	--
01	x	Mid	1	CPU	Down	USB	NA	SRC/PCI33	Down
10	0	High	2	CPU	Center	USB	NA	SRC/PCI33	Down
11	1	High	3	CPU	Center	USB/25M	NA	SRC/PCI33	Down

Pin No.	Name	Type	Description
6	PCI4/SRC5_EN	I/O, SE	3.3V tolerant input to enable SRC5/3.3V, 33MHz clock. *(Sampled on the CKPWRGD assertion)* 1 = SRC5, 0 = CPU_STP#
7	PCIF/ITP_EN	I/O, SE	3.3V LVTTL input to enable SRC8 or CPU2_ITP/3.3V, 33MHz clock. *(Sampled on the CKPWRGD assertion)* 1 = CPU2_ITP, 0 = SRC8
8	VSS_PCI	GND	Ground for outputs.
9	VDD_48	PWR	3.3V Power supply for outputs and PLL.
10	USB_48/FSA	I/O	3.3V tolerant input for CPU frequency selection/fixed 3.3V, 48MHz clock output. *(Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications)*
11	VSS_48	GND	Ground for outputs.
12	VDD_IO	PWR	0.7V Power supply for outputs.
13	SRC0/DOT96	O, DIF	100MHz Differential serial reference clocks/Fixed 96MHz clock output. *(Selected via I2C default is SRC0)*
14	SRC0#/DOT96#	O, DIF	100MHz Differential serial reference clocks/Fixed 96MHz clock output. *(Selected via I2C default is SRC0)*
15	VSS_IO	GND	Ground for PLL2.
16	VDD_PLL3	PWR	3.3V Power supply for PLL3
17	SRC1/LCD100/SE1	O, DIF, SE	100MHz Differential serial reference clocks/100MHz LCD video clock/SE1 clocks. *(Default SRC1, 100MHz clock)*
18	SRC1#/LCD100#/SE2	O, DIF, SE	100MHz Differential serial reference clocks/100MHz LCD video clock/SE2 clocks. *(Default SRC1, 100MHz clock)*
19	VSS_PLL3	GND	Ground for PLL3.
20	VDD_PLL3_IO	PWR	IO Power supply for PLL3 outputs.
21	SRC2/SATA	O, DIF	100MHz Differential serial reference clocks.
22	SRC2#/SATA#	O, DIF	100MHz Differential serial reference clocks.
23	VSS_SRC	GND	Ground for outputs.
24	SRC3/OE#_0/2_B	I/O, Dif	100MHz Differential serial reference clocks / 3.3V OE#_0/2_B, input, mappable via I2C to control either SRC0 or SRC2. *(Default SRC3, 100MHz clock)*
25	SRC3#OE#_1/4_B	I/O, Dif	100MHz Differential serial reference clocks / 3.3V OE#_1/4_B input, mappable via I2C to control either SRC1 or SRC4. *(Default SRC3, 100MHz clock)*

64 TSSOP Pin Definition (continued)

Pin No.	Name	Type	Description
26	VDD_SRC_IO	PWR	IO power supply for SRC outputs.
27	SRC4	O, DIF	100MHz Differential serial reference clocks.
28	SRC4#	O, DIF	100MHz Differential serial reference clocks.
29	VSS_SRC	GND	Ground for outputs.
30	SRC9	O, DIF	100MHz Differential serial reference clocks.
31	SRC9#	O, DIF	100MHz Differential serial reference clocks.
32	SRC11#/OE#_9	I/O, Dif	100MHz Differential serial reference clocks/3.3V OE#9 Input controlling SRC9 *(Default SRC11, 100MHz clock)*
33	SRC11/OE#_10	I/O, Dif	100MHz Differential serial reference clocks/3.3V OE#10 Input controlling SRC10. *(Default SRC11, 100MHz clock)*
34	SRC10	O, DIF	100MHz Differential serial reference clocks.
35	SRC10#	O, DIF	100MHz Differential serial reference clocks.
36	VDD_SRC_IO	PWR	IO Power supply for SRC outputs.
37	SRC5#CPU_STP#	I/O, Dif	3.3V tolerant input for stopping CPU outputs/100MHz Differential serial reference clocks.
38	SRC5/PCI_STP#	I/O, Dif	3.3V tolerant input for stopping PCI and SRC outputs/100MHz Differential serial reference clocks.
39	VDD_SRC	PWR	3.3V Power supply for SRC PLL.
40	SRC6#	O, DIF	100MHz Differential serial reference clocks.
41	SRC6	O, DIF	100MHz Differential serial reference clocks.
42	VSS_SRC	GND	Ground for outputs.
43	SRC7#/OE#_6	I/O, Dif	100MHz Differential serial reference clocks/3.3V OE#6 Input controlling SRC6. *(Default SRC7, 100MHz clock).*
44	SRC7/OE#_8	I/O, Dif	100MHz Differential serial reference clocks/3.3V OE#8 Input controlling SRC8. *(Default SRC7, 100MHz clock).*
45	VDD_SRC_IO	PWR	0.7V power supply for SRC outputs.
46	SRC8#/CPU2#_ITP#	O, DIF	Selectable differential CPU or SRC clock output. ITP_EN = 0 at CKPWRGD assertion = SRC8 ITP_EN = 1 @ CKPWRGD assertion = CPU2 *(Note: CPU2 is an iAMT clock in iAMT mode depending on the configuration set in Byte 11 Bit3:2)*
47	SRC8/CPU2_ITP	O, DIF	Selectable differential CPU or SRC clock output. ITP_EN = 0 at CKPWRGD assertion = SRC8 ITP_EN = 1 @ CKPWRGD assertion = CPU2 *(Note: CPU2 is an iAMT clock in iAMT mode depending on the configuration set in Byte 11 Bit3:2)*
48	IO_VOUT	PWR	Integrated Linear Regulator Control.
49	VDD_CPU_IO	PWR	IO Power supply for CPU outputs.
50	CPU1#	O, DIF	Differential CPU clock outputs. *(Note: CPU1 is an iAMT clock in iAMT mode depending on the configuration set in Byte 11 Bit3:2)*
51	CPU1	O, DIF	Differential CPU clock outputs. *(Note: CPU1 is an iAMT clock in iAMT mode depending on the configuration set in Byte 11 Bit3:2)*
52	VSS_CPU	GND	Ground for outputs.
53	CPU#0	O, DIF	Differential CPU clock outputs.
54	CPU0	O, DIF	Differential CPU clock outputs.
55	VDD_CPU	PWR	3.3V Power supply for CPU PLL.
56	CKPWRGD/PD#	I	3.3V LVTTL input. This pin is a level sensitive strobe used to latch the FS_A, FS_B, FS_C, FS_D, SRC5_SEL, and ITP_EN. After CKPWRGD (active HIGH) assertion, this pin becomes a real-time input for asserting power down (active LOW).

64 TSSOP Pin Definition (continued)

Pin No.	Name	Type	Description
57	FSB/TEST_MODE	I	3.3V tolerant input for CPU frequency selection. Selects Ref/N or Tri-state when in test mode 0 = Tri-state, 1 = Ref/N. *Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications.*
58	VSS_REF	GND	Ground for outputs.
59	XOUT	O, SE	14.318MHz Crystal output. *(Float XOUT if using CLKIN)*
60	XIN/CLKIN	I	14.318MHz Crystal input or 3.3V, 14.318MHz input clock signal.
61	VDD_REF	PWR	3.3V Power supply for outputs and also maintains SMBUS registers during power-down.
62	REF0/FSC/TEST_SEL	I/O	3.3V tolerant input for CPU frequency selection/fixed 14.318MHz clock output. Selects test mode if pulled to V_{IHFS_C} when CKPWRGD is asserted HIGH. *Refer to DC Electrical Specifications table for* V_{ILFS_C}, V_{IMFS_C}, V_{IHFS_C} *specifications.*
63	SMB_DATA	I/O	SMBus compatible SDATA.
64	SMB_CLK	I	SMBus compatible SCLOCK.

Table 1. Frequency Select Pin (FSA, FSB and FSC)

FSC	FSB	FSA	CPU	SRC	PCIF/PCI	27MHz	REF	DOT96	USB
0	0	0	266MHz						
0	0	1	133MHz						
0	1	0	200MHz						
0	1	1	166MHz	100MHz	33MHz	27MHz	14.318MHz	96MHz	48MHz
1	0	0	333MHz						
1	0	1	100MHz						
1	1	0	400MHz						
1	1	1	200MHz						

Frequency Select Pin (FSA, FSB and FSC)

Apply the appropriate logic levels to FSA, FSB, and FSC inputs before CKPWRGD assertion to achieve host clock frequency selection. When the clock chip sampled HIGH on CKPWRGD and indicates that VTT voltage is stable then FSA, FSB, and FSC input values are sampled. This process employs a one-shot functionality and once the CKPWRGD sampled a valid HIGH, all other FSA, FSB, FSC, and CKPWRGD transitions are ignored except in test mode.

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers are individually enabled or disabled. The registers associated with the Serial Data Interface initialize to

their default setting at power-up. The use of this interface is optional. Clock device register changes are normally made at system initialization, if any are required. The interface cannot be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, access the bytes in sequential order from lowest to highest (most significant bit first) with the ability to stop after any complete byte is transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code described in *Table 2*.

The block write and block read protocol is outlined in *Table 3* while *Table 4* outlines byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

Table 2. Command Code Definition

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000'

Table 3. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Byte Count–8 bits	20	Repeat start
28	Acknowledge from slave	27:21	Slave address–7 bits
36:29	Data byte 1–8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2–8 bits	37:30	Byte Count from slave–8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte /Slave Acknowledges	46:39	Data byte 1 from slave–8 bits
....	Data Byte N–8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave–8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave / Acknowledge
		....	Data Byte N from slave–8 bits
		....	NOT Acknowledge
		....	Stop

Table 4. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte–8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address–7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave–8 bits
		38	NOT Acknowledge
		39	Stop

Control Registers

Byte 0: Control Register 0

Bit	@Pup	Name	Description
7	HW	FS_C	CPU Frequency Select Bit, set by HW
6	HW	FS_B	CPU Frequency Select Bit, set by HW
5	HW	FS_A	CPU Frequency Select Bit, set by HW
4	0	iAMT_EN	Set via SMBus or by combination of PWRDWN, CPU_STP, and PCI_STP 0 = Legacy Mode, 1 = iAMT Enabled, Sticky 1
3	0	RESERVED	RESERVED
2	0	SRC_MAIN_SEL	Select source for SRC clock, 0 = SRC_MAIN = PLL1, PLL3_CFB Table applies 1 = SRC_MAIN = PLL3, PLL3_CFB Table does not apply
1	0	SATA_SEL	Select source of SATA clock 0 = SATA SRC_MAIN, 1= SATA PLL2
0	1	PD_Restore	Save Config. In powerdown 0 = Config. Cleared, 1 = Config. Saved

Byte 1: Control Register 1

Bit	@Pup	Name	Description
7	0	SRC0_SEL	Select for SRC0 or DOT96, 0 = SRC0, 1 = DOT96
6	0	PLL1_SS_DC	Select for down or center SS, 0 = Down spread, 1 = Center spread
5	0	PLL3_SS_DC	Select for down or center SS, 0 = Down spread, 1 = Center spread
4	0	PLL3_CFB3	Bit 4:1 only apply when SRC_SEL=0
3	0	PLL3_CFB2	0000 = PLL3 Disable Default PLL3 OFF, SRC1 = SRC_MAIN 0001 = 100 MHz 0.5% SSC Stby PLL3 ON, SRC1 = SRC_MAIN
2	0	PLL3_CFB1	0010 = 100 MHz 0.5% SSC Only SRC1 sourced from PLL3
1	1	PLL3_CFB0	0011 = 100 MHz 1.0% SSC Only SRC1 sourced from PLL3 0100 = 100 MHz 1.5% SSC Only SRC1 sourced from PLL3 0101 = 100 MHz 2.0% SSC Only SRC1 sourced from PLL3 0110 = RESERVED *Note: SE clocks required to be* 0111 = RESERVED *enabled through Byte 8 Bit[1:0]* 1000 = 1394A(24.576M) on SE1 and SE2 1001 = 1394A(24.576M) on SE1 and 1394B (98.304M) on SE2 1010 = 1394B on SE1 and SE2 1011 = 27MHz_NSS on SE1 and SE2 1100 = 25MHz on SE1 and SE2 1101 = 25MHz on SE1 and SE2 Disabled *(set whenPCI3/CFB0 is set high to config to HW mode 3)* 1110 = RESERVED 1111 = RESERVED
0	1	PCI_SEL	Select PCI Clock source from PLL1 or SRC_MAIN 0 = PLL1, 1 = SRC_MAIN

Byte 2: Control Register 2

Bit	@Pup	Name	Description
7	1	REF_OE	Output enable for REF 0 = Output Disabled, 1 = Output Enabled
6	1	USB_OE	Output enable for USB 0 = Output Disabled, 1 = Output Enabled

Byte 2: Control Register 2 (continued)

Bit	@Pup	Name	Description
5	1	PCIF0_OE	Output enable for PCIF0 0 = Output Disabled, 1 = Output Enabled
4	1	PCI4_OE	Output enable for PCI4 0 = Output Disabled, 1 = Output Enabled
3	1	PCI3_OE	Output enable for PCI3 0 = Output Disabled, 1 = Output Enabled
2	1	PCI2_OE	Output enable for PCI2 0 = Output Disabled, 1 = Output Enabled
1	1	PCI1_OE	Output enable for PCI1 0 = Output Disabled, 1 = Output Enabled
0	1	PCI0_OE	Output enable for PCI0 0 = Output Disabled, 1 = Output Enabled

Byte 3: Control Register 3

Bit	@Pup	Name	Description
7	1	SRC11_OE	Output enable for SRC11 0 = Output Disabled, 1 = Output Enabled
6	1	SRC10_OE	Output enable for SRC10 0 = Output Disabled, 1 = Output Enabled
5	1	SRC9_OE	Output enable for SRC9 0 = Output Disabled, 1 = Output Enabled
4	1	SRC8/ITP_OE	Output enable for SRC8 or ITP, 0 = Output Disabled, 1 = Output Enabled
3	1	SRC7_OE	Output enable for SRC7 0 = Output Disabled, 1 = Output Enabled
2	1	SRC6_OE	Output enable for SRC6 0 = Output Disabled, 1 = Output Enabled
1	1	SRC5_OE	Output enable for SRC5 0 = Output Disabled, 1 = Output Enabled
0	1	SRC4_OE	Output enable for SRC4 0 = Output Disabled, 1 = Output Enabled

Byte 4: Control Register 4

Bit	@Pup	Name	Description
7	1	SRC3_OE	Output enable for SRC3 0 = Output Disabled, 1 = Output Enabled
6	1	SRC2/SATA_OE	Output enable for SATA/SRC2 0 = Output Disabled, 1 = Output Enabled
5	1	SRC1_OE	Output enable for SRC 0 = Output Disabled, 1 = Output Enabled
4	1	SRC0/DOT96_OE	Output enable for SRC0/DOT96 0 = Output Disabled, 1 = Output Enabled
3	1	CPU1_OE	Output enable for CPU1 0 = Output Disabled, 1 = Output Enabled
2	1	CPU0_OE	Output enable for CPU0 0 = Output Disabled, 1 = Output Enabled
1	1	PLL1_SS_EN	Enable PLL1's spread modulation, 0 = Spread Disabled 1 = Spread Enabled
0	1	PLL3_SS_EN	Enable PLL3's spread modulation 0 = Spread Disabled, 1 = Spread Enabled

Byte 5: Control Register 5

Bit	@Pup	Name	Description
7	0	OE#_0/2_EN_A	Enable OE#_0/2 (clk req) 0 = Disabled OE#_0/2, 1 = Enabled OE#_0/2,
6	0	OE#_0/2_SEL_A	Set OE#_0/2 → SRC0 or SRC2 0 = OE#_0/2→SRC0, 1 = OE#_0/2→SRC2
5	0	OE#_1/4_EN_A	Enable OE#_1/4 (clk req) 0 = Disabled OE#_1/4, 1 = Enabled OE#_1/4,
4	0	OE#_1/4_SEL_A	Set OE#_1/4 → SRC1 or SRC4 0 = OE#_1/4→SRC1, 1 = OE#_1/4→SRC4
3	0	OE#_0/2_EN_B	Enable OE#_0/2 (clk req) 0 = Disabled OE#_0/2 1 = Enabled OE#_0/2
2	0	OE#_0/2_SEL_B	Set OE#_0/2 → SRC0 or SRC2 0 = OE#_0/2→SRC0, 1 = OE#_0/2→SRC2
1	0	OE#_1/4_EN_B	Enable OE#_1/4 (clk req) 0 = Disabled OE#_1/4, 1 = Enabled OE#_1/4,
0	0	OE#_1/4_SEL_B	Set OE#_1/4 → SRC1 or SRC4 0 = OE#_1/4→SRC1, 1 = OE#_1/4→SRC4

Byte 6: Control Register 6

Bit	@Pup	Name	Description
7	0	OE#_6_EN	Enable OE#_6 (clk req) → SRC6
6	0	OE#_8_EN	Enable OE#_8 (clk req) → SRC8
5	0	OE#_9_EN	Enable OE#_9 (clk req) → SRC9
4	0	OE#_10_EN	Enable OE#_10 (clk req) → SRC10
3	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED
1	0	LCD_100_STP_CTRL	Allows control of LCD_100 with assertion of PCI_STP# 0 = Free runningLCD_100, 1 = Stopped with PCI_STP#
0	0	SRC_STP_CTRL	Allows control of SRC with assertion of PCI_STP# 0 = Free running SRC 1 = Stopped with PCI_STP#

Byte 7: Vendor ID

Bit	@Pup	Name	Description
7	0	Rev Code Bit 3	Revision Code Bit 3
6	0	Rev Code Bit 2	Revision Code Bit 2
5	0	Rev Code Bit 1	Revision Code Bit 1
4	1	Rev Code Bit 0	Revision Code Bit 0
3	1	Vendor ID bit 3	Vendor ID Bit 3
2	0	Vendor ID bit 2	Vendor ID Bit 2
1	0	Vendor ID bit 1	Vendor ID Bit 1
0	0	Vendor ID bit 0	Vendor ID Bit 0

Byte 8: Control Register 8

Bit	@Pup	Name	Description
7	0	Device_ID3	0000 = CK505 Yellow Cover Device, 56-pin TSSOP
7	0	Device_ID2	0001 = CK505 Yellow Cover Device, 64-pin TSSOP 0010 = CK505 Yellow Cover Device, 48-pin QFN (reserved)
5	0	Device_ID1	0011 = CK505 Yellow Cover Device, 56-pin QFN (reserved)
4	1	Device_ID0	0100 = CK505 Yellow Cover Device, 64-pin QFN (reserved) 0101 = CK505 Yellow Cover Device, 72-pin QFN (reserved) 0110 = CK505 Yellow Cover Device, 48-pin SSOP (reserved) 0111 = CK505 Yellow Cover Device, 56-pin SSOP (reserved) 1000 = Reserved 1001 = Reserved 1010 = Reserved 1011 = Reserved 1100 = Reserved 1101 = Reserved 1110 = Reserved 1111 = Reserved
3	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED
1	0	SE1_OE	SE1 Output enable 0 = Output Disabled, 1 = Output Enabled
0	0	SE2_OE	SE2 Output enable 0 = Output Disabled, 1 = Output Enabled

Byte 9: Control Register 9

Bit	@Pup	Name	Description
7	0	PCIF0_STP_CTRL	Allows control of PCIF0 with assertion of PCI_STP# 0 = Free running PCIF, 1 = Stopped with PCI_STP#
6	HW_Pin	TME_STRAP	Trusted mode enable strap status, 0 = normal, 1 = no overclocking
5	1	REF_Bit1	REF drive strength control, *See Byte 18 for more setting* 0 = Low, 1 = High
4	0	TEST_MODE_SEL	Mode select either REF/N or tri-state 0 = All output tri-state, 1 = All output REF/N
3	0	TEST_MODE_ENTRY	Allow entry into test mode 0=Normal operation, 1=Enter test mode
2	1	IO_VOUT2	IO_VOUT[2,1,0]
1	0	IO_VOUT1	000 = 0.3V 001 = 0.4V
0	1	IO_VOUT0	010 = 0.5V 011 = 0.6V 100 = 0.7V 101 = 0.8V, *Default* 110 = 0.9V 111 = 1.0V

Byte 10: Control Register 10

Bit	@Pup	Name	Description
7	HW	SRC5_EN_STRAP	Read only bit for SRC5_EN_STRAP 0 = CPU/PCI_STP enabled, 1 = SRC5 pair enabled
6	1	PLL3_EN	PLL3 Enabled 0 = PLL3 disabled, 1 = PLL3 enabled
5	1	PLL2_EN	PLL2 Enabled 0 = PLL2 disabled, 1 = PLL2 enabled
4	1	SRC_DIV_EN	SRC Divider Enabled 0 = SRC Divider disabled, 1 = SRC Divider enabled

Byte 10: Control Register 10 (continued)

Bit	@Pup	Name	Description
3	1	PCI_DIV_EN	PCI Divider Enabled 0 = PCI Divider disabled, 1 = PCI Divider enabled
2	1	CPU_DIV_EN	CPU Divider Enabled 0 = CPU Divider disabled, 1 = CPU Divider enabled
1	1	CPU1_STP_CRTL	Allow control of CPU1 with assertion of CPU_STP# 0 = Free running, 1 = Stopped with CPU_STP#
0	1	CPU0_STP_CRTL	Allow control of CPU0 with assertion of CPU_STP# 0 = Free running, 1 = Stopped with CPU_STP#

Byte 11: Control Register 11

Bit	@Pup	Name	Description
7	HW	PCI3_CFG1	
6	HW	PCI3_CFG0	<table><tr><th>CFG [1:0]</th><th>PCI2/TME</th><th>PCI3/CGF0</th><th>Mode</th><th colspan="2">PLL1</th><th colspan="2">PLL2</th><th colspan="2">PLL3</th></tr><tr><th></th><th></th><th></th><th></th><th>Output</th><th>SSC</th><th>Output</th><th>SSC</th><th>Output</th><th>SSC</th></tr><tr><td>00</td><td>x</td><td>Low</td><td>0 -Def</td><td>CPU / SRC / PCI33</td><td>Down</td><td>USB</td><td>NA</td><td>--</td><td>--</td></tr><tr><td>01</td><td>x</td><td>Mid</td><td>1</td><td>CPU</td><td>Down</td><td>USB</td><td>NA</td><td>SRC/PCI33</td><td>Down</td></tr><tr><td>10</td><td>0</td><td>High</td><td>2</td><td>CPU</td><td>Center</td><td>USB</td><td>NA</td><td>SRC/PCI33</td><td>Down</td></tr><tr><td>11</td><td>1</td><td>High</td><td>3</td><td>CPU</td><td>Center</td><td>USB/25M</td><td>NA</td><td>SRC/PCI33</td><td>Down</td></tr></table>
5	0	25MHz_EN_SE1	25MHz Output Enabled applies to Powerdown / M1 *(Only applies when PCI3/CGFG0 strap is set high to enter HW mode 3)* 0 = 25MHz disabled in Powerdown / M1 1 = 25MHz enabled in Powerdown / M1; Sticky 1
4	1	RESERVED	RESERVED
3	0	CPU2_AMT_EN	
2	1	CPU1_AMT_EN	<table><tr><th>PCIF0/ITP_EN</th><th>AMT_EN</th><th>CPU2_AMT_EN</th><th>CPU1_AMT_EN</th><th>Description</th></tr><tr><td>x</td><td>1</td><td>0</td><td>0</td><td>Reserved</td></tr><tr><td>x</td><td>1</td><td>0</td><td>1</td><td>CPU1 = M1 Clock</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>CPU2 - M1 Clock</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>CPU1 and CPU2 = M1 Clock</td></tr></table>
1	1	PCI-E_GEN2	PCI-E_Gen2 Compliant (Read Only) 0 = non Gen2, 1= Gen2 Compliant
0	1	CPU2_STP_CRTL	Allow control of CPU2 with assertion of CPU_STP# 0 = Free running, 1 = Stopped with CPU_STP#

Byte 12: Byte Count

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	0	BC5	Byte count
4	0	BC4	Byte count
3	1	BC3	Byte count
2	1	BC2	Byte count
1	0	BC1	Byte count
0	1	BC0	Byte count

Byte 13: Control Register 13

Bit	@Pup	Name	Description
7	1	USB_Bit1	USB drive strength control, *See Byte 18 for more setting* 0 = Low, 1= High
6	1	PCI/PCIF_Bit1	PCI drive strength control, *See Byte 18 for more setting* 0 = Low, 1 = High
5	0	PLL1_Spread	Select percentage of spread for PLL1 0 = 0.5%, 1=0.45%
4	0	SATA_SS_EN	Enable SATA spread modulation, 0 = Spread Disabled 1 = Spread Enabled
3	1	EN_CFG0_SET	By defalult CFG0 pin strap sets the SMBus initial values to select the HW mode. When this bit is written0, subsequent SMBus accesses is the Lathes Open state, can overwrite the CFG0 pin setting into the SMBus bits and set the mode before the M0 state: specifically B0b2, B1b[6,4,3], B9b1, B11b5
2	1	SE1/SE2_Bit1	SE1 and SE2 drive strength control, *See Byte 18 for more setting* 0 = Low, 1 = High
1	1	RESERVED	RESERVED
0	1	SW_PCI	SW PCI_STP# Function 0 = SW PCI_STP assert, 1 = SW PCI_STP deassert When this bit is set to 0, all STOPPABLE PCI, PCIF and SRC outputs will be stopped in a synchronous manner with no short pulses. When this bit is set to 1, all STOPPED PCI, PCIF and SRC outputs will resume in a synchronous manner with no short pulses.

Byte 14: Control Register 14

Bit	@Pup	Name	Description
7	0	CPU_DAF_N7	If Prog_CPU_EN is set, the values programmed in CPU_DAF_N[8:0] and CPU_DAF_M[6:0] will be used to determine the CPU output frequency. The setting of the FS_Override bit determines the frequency ratio for CPU and other output clocks. When it is cleared, the same frequency ratio stated in the Latched FS[C:A] register will be used. When it is set, the frequency ratio stated in the FSEL[2:0] register will be used
6	0	CPU_DAF_N6	
5	0	CPU_DAF_N5	
4	0	CPU_DAF_N4	
3	0	CPU_DAF_N3	
2	0	CPU_DAF_N2	
1	0	CPU_DAF_N1	
0	0	CPU_DAF_N0	

Byte 15: Control Register 15

Bit	@Pup	Name	Description
7	0	CPU_DAF_N8	See Byte 14 for description
6	0	CPU_DAF_M6	If Prog_CPU_EN is set, the values programmed are in CPU_FSEL_N[8:0] and CPU_FSEL_M[6:0] will be used to determine the CPU output frequency. The setting of the FS_Override bit determines the frequency ratio for CPU and other output clocks. When it is cleared, the same frequency ratio stated in the Latched FS[C:A] register will be used. When it is set, the frequency ratio stated in the FSEL[2:0] register will be used
5	0	CPU_DAF_M5	
4	0	CPU_DAF_M4	
3	0	CPU_DAF_M3	
2	0	CPU_DAF_M2	
1	0	CPU_DAF_M1	
0	0	CPU_DAF_M0	

Byte 16: Control Register 16

Bit	@Pup	Name	Description

Byte 16: Control Register 16

7	0	PCI-E_N7	If Prog_SRC_EN is set, the values programmed in SRC_DAF_N[7:0] will
6	0	PCI-E_N6	be used to determine the SRC output frequency.
5	0	PCI-E_N5	
4	0	PCI-E_N4	
3	0	PCI-E_N3	
2	0	PCI-E_N2	
1	0	PCI-E_N1	
0	0	PCI-E_N0	

Byte 17: Control Register 17

Bit	@Pup	Name	Description
7	0	SMSW_EN	Enable Smooth Switching, 0 = Disabled, 1= Enabled
6	0	SMSW_SEL	Smooth switch select, 0 = CPU_PLL, 1 = SRC_PLL
5	0	RESERVED	RESERVED
4	0	Prog_PCI-E_EN	Programmable PCI-E frequency enable 0 = Disabled, 1= Enabled
3	0	Prog_CPU_EN	Programmable CPU frequency enable 0 = Disabled, 1= Enabled
2	0	RESERVED	RESERVED
1	0	RESERVED	RESERVED
0	0	RESERVED	RESERVED

Byte 18: Control Register 18

Bit	@Pup	Name	Description			
7	0	PCIF/PCI_Bit2	Drive Strength Control - Bit[2:0]			
6	1	PCIF/PCI_Bit0		Bit 2 (Byte18)	Bit 1 (Various Bytes)	Bit 0 (Byte 18)	Buffer Strength
5	0	USB_Bit2		1	1	1	Strongest
4	0	USB_Bit0		1	1	0	
3	0	SE1/SE2_Bit2		1	0	1	
2	0	SE1/SE2_Bit0		1	0	0	
1	0	REF_Bit2	Default PCI	0	1	1	
0	0	REF_Bit0	Default REF/Usb	0	1	0	
				0	0	1	
				0	0	0	Weakest

Table 5. Output Driver Status during PCI-STP# and CPU-STP#

		PCI_STP# Asserted	CPU_STP# Asserted	SMBus OE Disabled
Single-ended Clocks	Stoppable	Driven low	Running	Driven low
	Non stoppable	Running	Running	
Differential Clocks	Stoppable	Clock driven high	Clock driven high	Clock driven Low or 20K pulldown
		Clock# driven low	Clock# driven low	
	Non stoppable	Running	Running	

Table 6. Output Driver Status

	All Single-ended Clocks		All Differential Clocks except CPU1		CPU1	
	w/o Strap	w/ Strap	Clock	Clock#	Clock	Clock#
Latches Open State	Low	Hi-z	Low or 20K pulldown	Low	Low or 20K pulldown	Low
Powerdown	Low	Hi-z	Low or 20K pulldown	Low	Low or 20K pulldown	Low
M1	Low	Hi-z	Low or 20K pulldown	Low	Running	Running

Dial-A-Frequency® (CPU andSRC)

This feature allows the user to over-clock their system by slowly stepping up the CPU or SRC frequency. When the programmable output frequency feature is enabled, the CPU and SRC frequencies are determined by the following equation:

Fcpu = G * N/M or Fcpu=G2 * N, where G2 = G / M.

- "N" and "M" are the values programmed in Programmable Frequency Select N-Value Register and M-Value Register, respectively.

- "G" stands for the PLL Gear Constant, which is determined by the programmed value of FS[E:A]. See *Table 1*, *Frequency Select Table* for the Gear Constant for each Frequency selection. The PCI Express only allows user control of the N register, the M value is fixed and documented in *Table 1*, *Frequency Select Table*.

In this mode, the user writes the desired N and M values into the DAF I2C registers. The user cannot change only the M value and must change both the M and the N values at the same time, if they require a change to the M value. The user may change only the N value.

Associated Register Bits

- *CPU_DAF Enable* – This bit enables CPU DAF mode. By default, it is not set. When set, the operating frequency is determined by the values entered into the CPU_DAF_N register. Note that the CPU_DAF_N and M register must contain valid values before CPU_DAF is set. Default = 0, (No DAF).

- *CPU_DAF_N* – There are nine bits (for 512 values) to linearly change the CPU frequency (limited by VCO range). Default = 0, (0000). The allowable values for N are detailed in *Table 1*, *Frequency Select Table*.

- *CPU DAF M* – There are 7 bits (for 128 values) to linearly change the CPU frequency (limited by VCO range). Default = 0, the allowable values for M are detailed in *Table 1*, *Frequency Select Table*

- *SRC_DAF Enable* – This bit enables SRC DAF mode. By default, it is not set. When set, the operating frequency is determined by the values entered into the SRC_DAF_N register. Note that the SRC_DAF_N register must contain valid values before SRC_DAF is set. Default = 0, (No DAF).

- *SRC_DAF_N* – There are nine bits (for 512 values) to linearly change the CPU frequency (limited by VCO range). Default = 0, (0000). The allowable values for N are detailed in *Table 1*, *Frequency Select Table*.

Smooth Switching

The device contains one smooth switch circuit that is shared by the CPU PLL and SRC PLL. The smooth switch circuit ensures that when the output frequency changes by overclocking, the transition from the old frequency to the new frequency is a slow, smooth transition containing no glitches. The rate of change of output frequency when using the smooth switch circuit is less than 1 MHz/0.667 μs. The frequency overshoot and undershoot is less than 2%.

The Smooth Switch circuit assigns auto or manual. In Auto mode, clock generator assigns smooth switch automatically when the PLL does overclocking. For manual mode, assign the smooth switch circuit to PLL via Smbus. By default the smooth switch circuit is set to auto mode. PLL can be over-clocked when it does not have control of the smooth switch circuit but it is not guaranteed to transition to the new frequency without large frequency glitches.

Do not enable over-clocking and change the N values of both PLLs in the same SMBUS block write and use smooth switch mechanism on spread spectrum on/off.

PD_RESTORE

If a '0' is set for Byte 0 bit 0 then, upon assertion of PD# LOW, the SL28506 initiates a full reset. The result of this is that the clock chip emulates a cold power on start and goes to the "Latches Open" state. If the PD_RESTORE bit is set to a '1' then the configuration is stored upon PD# asserted LOW. Note that if the iAMT bit, Byte 0 bit 3, is set to a '1' then the PD_RE-STORE bit must be ignored. In other words, in Intel iAMT mode, PD# reset is not allowed.

PD# (Power down) Clarification

The CKPWRGD/PD# pin is a dual-function pin. During initial power up, the pin functions as CKPWRGD. Once CKPWRGD has been sampled HIGH by the clock chip, the pin assumes PD# functionality. The PD# pin is an asynchronous active LOW input used to shut off all clocks cleanly before shutting off power to the device. This signal is synchronized internally to the device before powering down the clock synthesizer. PD# is also an asynchronous input for powering up the system. When PD# is asserted LOW, clocks are driven to a LOW value and held before turning off the VCOs and the crystal oscillator.

PD# (Power down) Assertion

When PD is sampled HIGH by two consecutive rising edges of CPUC, all single-ended outputs will be held LOW on their next HIGH-to-LOW transition and differential clocks must held LOW. When PD mode is desired as the initial power on state, PD must be asserted HIGH in less than 10 μs after asserting CKPWRGD.

PD# Deassertion

The power up latency is less than 1.8 ms. This is the time from the deassertion of the PD# pin or the ramping of the power supply until the time that stable clocks are generated from the clock chip. All differential outputs stopped in a three-state condition, resulting from power down are driven high in less than 300 µs of PD# deassertion to a voltage greater than 200 mV. After the clock chip's internal PLL is powered up and locked, all outputs are enabled within a few clock cycles of each clock. *Figure 2* is an example showing the relationship of clocks coming up.
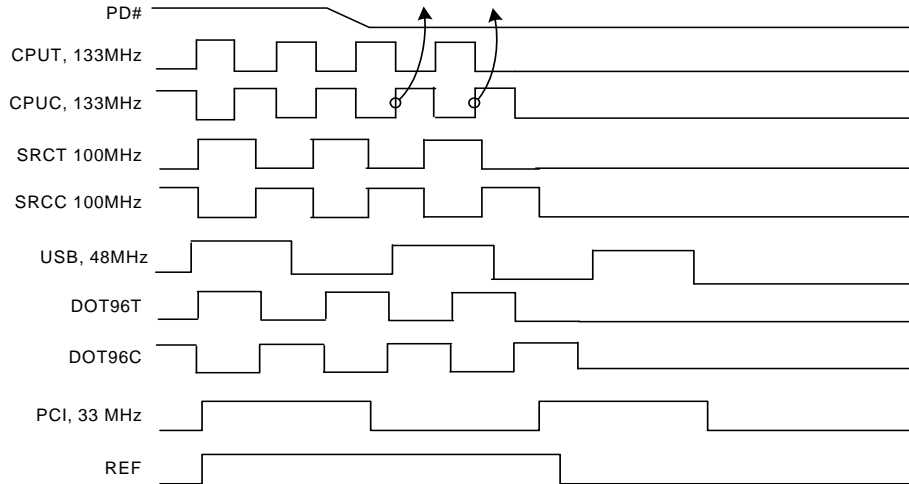
Figure 1. Power down Assertion Timing Waveform
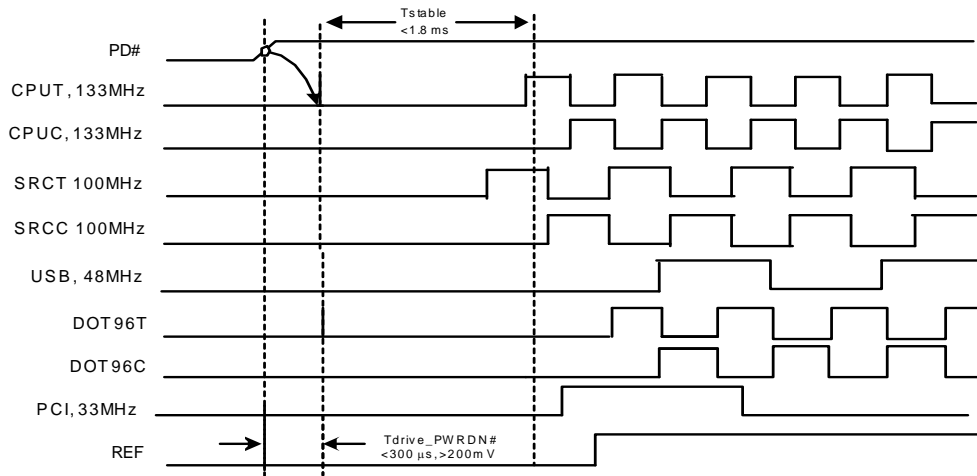
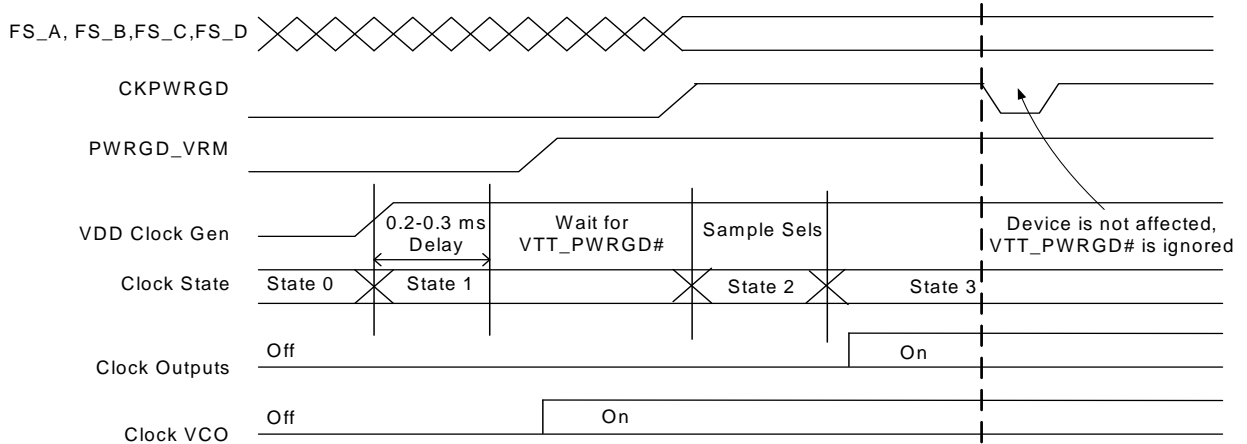**Figure 2. Power down Deassertion Timing Waveform**

Figure 3. CKPWRGD Timing Diagram

CPU_STP# Assertion

The CPU_STP# signal is an active LOW input used for synchronous stopping and starting the CPU output clocks while the rest of the clock generator continues to function. When the CPU_STP# pin is asserted, all CPU outputs that are set with the SMBus configuration to be stoppable are stopped within two to six CPU clock periods after sampled by two rising edges of the internal CPUC clock. The final states of the stopped CPU signals are CPUT = HIGH and CPUC = LOW.

CPU_STP# Deassertion

The deassertion of the CPU_STP# signal causes all stopped CPU outputs to resume normal operation in a synchronous manner. No short or stretched clock pulses are produced when the clock resumes. The maximum latency from the deassertion to active outputs is no more than two CPU clock cycles.
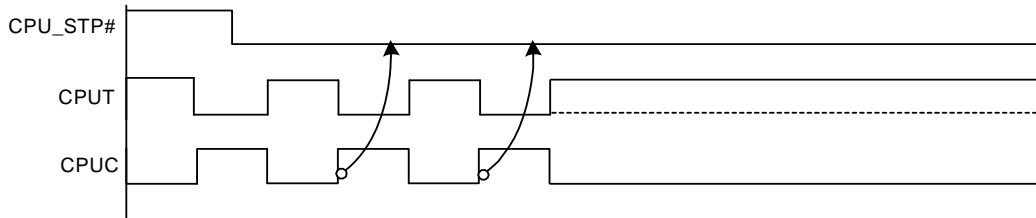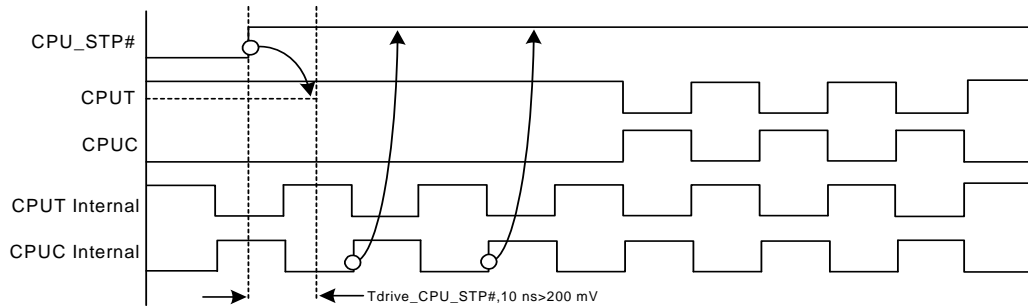
Figure 4. CPU_STP# Assertion Waveform

Figure 5. CPU_STP# Deassertion Waveform

PCI_STP# Assertion

The PCI_STP# signal is an active LOW input used for synchronously stopping and starting the PCI outputs while the rest of the clock generator continues to function. The set-up time for capturing PCI_STP# going LOW is 10 ns (t_{SU}). (See *Figure 6.*) The PCIF clocks are affected by this pin if their corresponding control bit in the SMBus register is set to allow them to be free running.
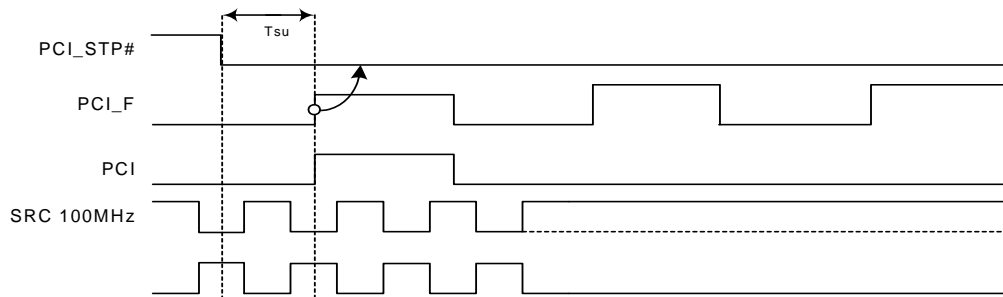
Figure 6. PCI_STP# Assertion Waveform

PCI_STP# Deassertion

The deassertion of the PCI_STP# signal causes all PCI and stoppable PCIF clocks to resume running in a synchronous manner within two PCI clock periods, after PCI_STP# transitions to a HIGH level.
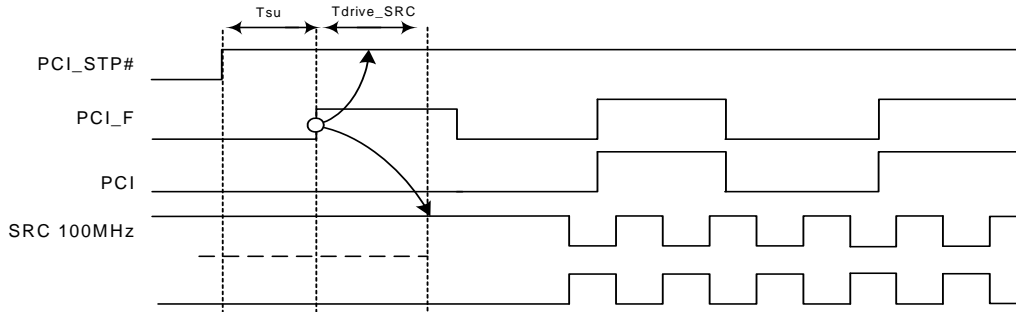

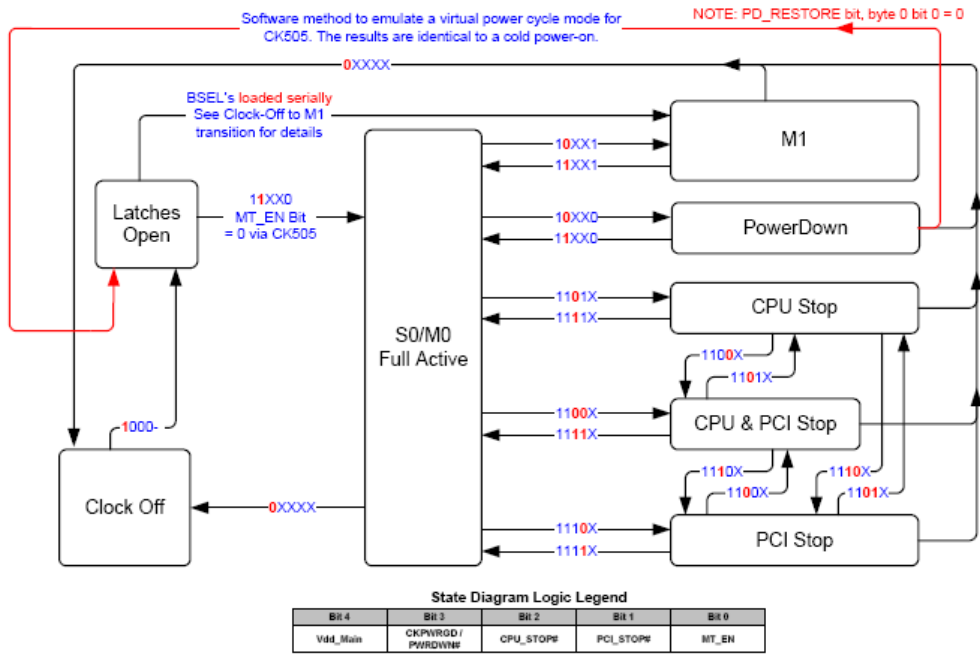**Figure 7. PCI_STP# Deassertion Waveform**
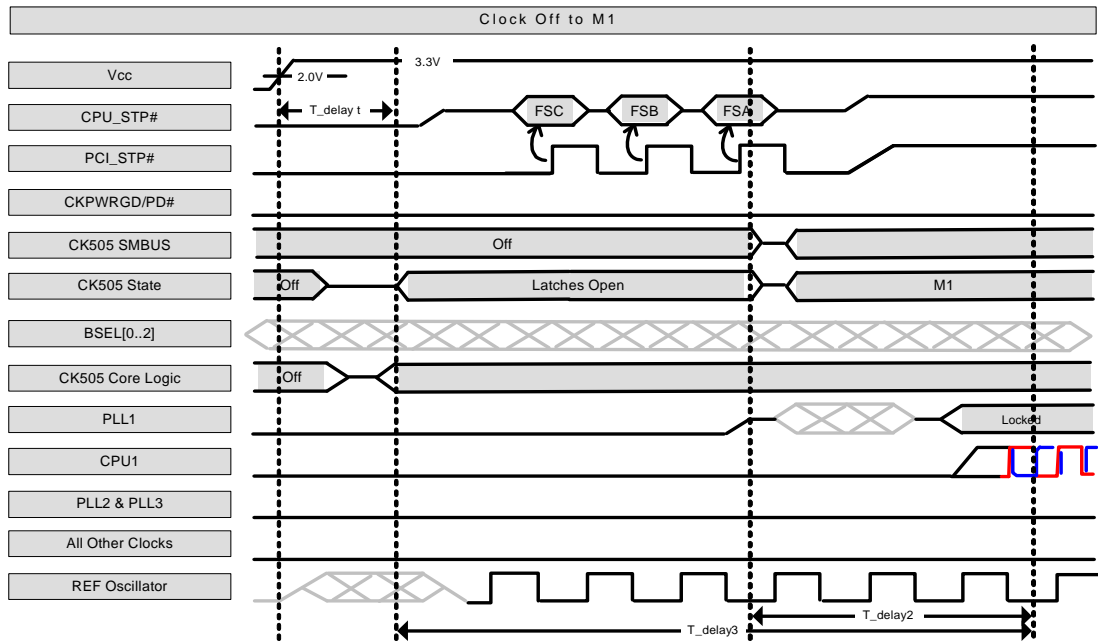

Figure 8. Clock Generator Power up/Run State Diagram

Figure 9. BSEL Serial Latching

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
$V_{DD\_3.3V}$	Supply Voltage	Functional	–	4.6	V
V_{DD_IO}	IO Supply Voltage	Functional		1.5	V
V_{IN}	Input Voltage	Relative to V_{SS}	–0.5	4.6	V_{DC}
T_S	Temperature, Storage	Non-functional	–65	150	°C
T_A	Commercial Temperature, Operating Ambient	Functional	0	85	°C
	Industrial Temperature, Operating Ambient		-40	+85	°C
T_J	Temperature, Junction	Functional	–	150	°C
$\emptyset_{JC}$	Dissipation, Junction to Case	JEDEC (JESD 51)	–	20	°C/W
$\emptyset_{JA}$	Dissipation, Junction to Ambient	JEDEC (JESD 51)	–	60	°C/W
ESD_{HBM}	ESD Protection (Human Body Model)	JEDEC (JESD 22-A114)	2000	–	V
UL-94	Flammability Rating	UL (CLASS)	V–0		
MSL	Moisture Sensitivity Level		1		

Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
VDD core	3.3V Operating Voltage	3.3 ± 5%	3.135	3.465	V
V_{IH}	3.3V Input High Voltage (SE)		2.0	V_{DD} + 0.3	V
V_{IL}	3.3V Input Low Voltage (SE)		V_{SS} – 0.3	0.8	V
V_{IHI2C}	Input High Voltage	SDATA, SCLK	2.2	–	V
V_{ILI2C}	Input Low Voltage	SDATA, SCLK	–	1.0	V
V_{IH_FS}	FS_[A,B] Input High Voltage		0.7	1.5	V
V_{IL_FS}	FS_[A,B] Input Low Voltage		V_{SS} – 0.3	0.35	V
$V_{IHFS\_C\_TEST}$	FS_C Input High Voltage		2	V_{DD} + 0.3	V
$V_{IMFS\_C\_NORMAL}$	FS_C Input Middle Voltage		0.7	1.5	V
$V_{ILFS\_C\_NORMAL}$	FS_C Input Low Voltage		V_{SS} – 0.3	0.35	V
PCI3/CFG0 $_{HIGH}$	PCI3/CFG0 Input High Voltage	Typ. 2.75V	2.40	VDD	V
PCI3/CFG0 $_{MID}$	PCI3/CFG0 Input Mid Voltage	Typ. 1.65V	1.30	2.00	V
PCI3/CFG0 $_{LOW}$	PCI3/CFG0 Input Low Voltage	Typ. 0.550V	0	0.900	V
I_{IH}	Input High Leakage Current	Except internal pull-down resistors, $0 < V_{IN} < V_{DD}$	–	5	µA
I_{IL}	Input Low Leakage Current	Except internal pull-up resistors, $0 < V_{IN} < V_{DD}$	–5	–	µA
V_{OH}	3.3V Output High Voltage (SE)	I_{OH} = –1 mA	2.4	–	V
V_{OL}	3.3V Output Low Voltage (SE)	I_{OL} = 1 mA	–	0.4	V
$V_{DD\ IO}$	Low Voltage IO Supply Voltage		1	3.465	V
I_{OZ}	High-impedance Output Current		–10	10	µA
C_{IN}	Input Pin Capacitance		1.5	5	pF
C_{OUT}	Output Pin Capacitance			6	pF
L_{IN}	Pin Inductance		–	7	nH
V_{XIH}	Xin High Voltage		$0.7V_{DD}$	V_{DD}	V
V_{XIL}	Xin Low Voltage		0	$0.3V_{DD}$	V

DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
IDD_{PWRDWN}	Power Down Current			1	mA
$I_{DD3.3V}$	Dynamic Supply Current		–	250	mA

AC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
Crystal					
L$_{ACC}$	Long-term Accuracy		–	300	ppm
Clock Input					
T$_{DC}$	CLKIN Duty Cycle	Measured at VDD/2	47	53	%
T$_R$/T$_F$	CLKIN Rise and Fall Times	Measured between 0.2V$_{DD}$ and 0.8V$_{DD}$	0.5	4.0	V/ns
T$_{CCJ}$	CLKIN Cycle to Cycle Jitter	Measured at VDD/2	–	250	ps
T$_{LTJ}$	CLKIN Long Term Jitter	Measured at VDD/2	–	350	ps
V$_{IL}$	Input Low Voltage	XIN / CLKIN pin	–	0.8	V
V$_{IH}$	Input High Voltage	XIN / CLKIN pin	2	VDD+0.3	V
I$_{IL}$	Input LowCurrent	XIN / CLKIN pin, 0 < VIN <0.8	–	20	uA
I$_{IH}$	Input HighCurrent	XIN / CLKIN pin, VIN = VDD	–	35	uA
CPU at 0.7V					
T$_{DC}$	CPU Clock Duty Cycle	Measured at 0V differential at 0.1s	**45**	**55**	%
T$_{PERIOD}$	100 MHz CPU Clock Period	Measured at 0V differential at 0.1s	**9.99900**	**10.00100**	ns
T$_{PERIOD}$	133 MHz CPU Clock Period	Measured at 0V differential at 0.1s	**7.49925**	**7.50075**	ns
T$_{PERIOD}$	166 MHz CPU Clock Period	Measured at 0V differential at 0.1s	**5.99940**	**6.00060**	ns
T$_{PERIOD}$	200 MHz CPU Clock Period	Measured at 0V differential at 0.1s	**4.99950**	**5.00050**	ns
T$_{PERIOD}$	266 MHz CPU Clock Period	Measured at 0V differential at 0.1s	**3.74963**	**3.75038**	ns
T$_{PERIOD}$	333 MHz CPU Clock Period	Measured at 0V differential at 0.1s	**2.99970**	**3.00030**	ns
T$_{PERIOD}$	400 MHz CPU Clock Period	Measured at 0V differential at 0.1s	**2.49975**	**2.50025**	ns
T$_{PERIODSS}$	100 MHz CPU Clock Period, SSC	Measured at 0V differential at 0.1s	**10.02406**	**10.02607**	ns
T$_{PERIODSS}$	133 MHz CPU Clock Period, SSC	Measured at 0V differential at 0.1s	**7.51804**	**7.51955**	ns
T$_{PERIODSS}$	166 MHz CPU Clock Period, SSC	Measured at 0V differential at 0.1s	**6.01444**	**6.01564**	ns
T$_{PERIODSS}$	200 MHz CPU Clock Period, SSC	Measured at 0V differential at 0.1s	**5.01203**	**5.01303**	ns
T$_{PERIODSS}$	266 MHz CPU Clock Period, SSC	Measured at 0V differential at 0.1s	**3.75902**	**3.75978**	ns
T$_{PERIODSS}$	333 MHz CPU Clock Period, SSC	Measured at 0V differential at 0.1s	**3.00722**	**3.00782**	ns
T$_{PERIODSS}$	400 MHz CPU Clock Period, SSC	Measured at 0V differential at 0.1s	**2.50601**	**2.50652**	ns
T$_{PERIODAbs}$	100 MHz CPU Clock Absolute period	Measured at 0V differential at 1 clock	**9.91400**	**10.0860**	ns
T$_{PERIODAbs}$	133 MHz CPU Clock Absolute period	Measured at 0V differential at 1 clock	**7.41425**	**7.58575**	ns
T$_{PERIODAbs}$	166 MHz CPU Clock Absolute period	Measured at 0V differential at 1 clock	**5.91440**	**6.08560**	ns
T$_{PERIODAbs}$	200 MHz CPU Clock Absolute period	Measured at 0V differential at 1 clock	**4.91450**	**5.08550**	ns
T$_{PERIODAbs}$	266 MHz CPU Clock Absolute period	Measured at 0V differential at 1 clock	**3.66463**	**3.83538**	ns
T$_{PERIODAbs}$	333 MHz CPU Clock Absolute period	Measured at 0V differential at 1 clock	**2.91470**	**3.08530**	ns
T$_{PERIODAbs}$	400 MHz CPU Clock Absolute period	Measured at 0V differential at 1 clock	**2.41475**	**2.58525**	ns
T$_{PERIODSSAbs}$	100 MHz CPU Clock Absolute period, SSC	Measured at 0V differential at 1 clock	**9.91406**	**10.1362**	ns
T$_{PERIODSSAbs}$	133 MHz CPU Clock Absolute period, SSC	Measured at 0V differential at 1 clock	**7.41430**	**7.62340**	ns
T$_{PERIODSSAbs}$	166 MHz CPU Clock Absolute period, SSC	Measured at 0V differential at 1 clock	**5.91444**	**6.11572**	ns
T$_{PERIODSSAbs}$	200 MHz CPU Clock Absolute period, SSC	Measured at 0V differential at 1 clock	**4.91453**	**5.11060**	ns
T$_{PERIODSSAbs}$	266 MHz CPU Clock Absolute period, SSC	Measured at 0V differential at 1 clock	**3.66465**	**3.85420**	ns
T$_{PERIODSSAbs}$	333 MHz CPU Clock Absolute period, SSC	Measured at 0V differential at 1 clock	**2.91472**	**3.10036**	ns

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
$T_{PERIODSSAbs}$	400 MHz CPU Clock Absolute period, SSC	Measured at 0V differential at 1 clock	2.41477	2.59780	ns
T_{CCJ}	CPU Cycle to Cycle Jitter	Measured at 0V differential	–	85	ps
T_{CCJ2}	CPU2_ITP Cycle to Cycle Jitter	Measured at 0V differential	–	125	ps
L_{ACC}	Long-term Accuracy	Measured at 0V differential	–	100	ppm
T_{SKEW}	CPU0 to CPU1 Clock Skew	Measured at 0V differential	–	100	ps
T_{SKEW2}	CPU2_ITP to CPU0 Clock Skew	Measured at 0V differential	–	150	ps
T_R / T_F	CPU Rising/Falling Slew rate	Measured differentially from ±150 mV	2.5	8	V/ns
T_{RFM}	Rise/Fall Matching	Measured single-endedly from ±75 mV	–	20	%
V_{HIGH}	Voltage High			1.15	V
V_{LOW}	Voltage Low		–0.3	–	V
V_{OX}	Crossing Point Voltage at 0.7V Swing		300	550	mV
SRC at 0.7V					
T_{DC}	SRC Duty Cycle	Measured at 0V differential	45	55	%
T_{PERIOD}	100 MHz SRC Period	Measured at 0V differential at 0.1s	9.99900	10.0010	ns
$T_{PERIODSS}$	100 MHz SRC Period, SSC	Measured at 0V differential at 0.1s	10.02406	10.02607	ns
$T_{PERIODAbs}$	100 MHz SRC Absolute Period	Measured at 0V differential at 1 clock	9.87400	10.1260	ns
$T_{PERIODSSAbs}$	100 MHz SRC Absolute Period, SSC	Measured at 0V differential at 1 clock	9.87406	10.1762	ns
$T_{SKEW(window)}$	Any SRC Clock Skew from the earliest bank to the latest bank	Measured at 0V differential	–	3.0	ns
T_{CCJ}	SRC Cycle to Cycle Jitter	Measured at 0V differential	–	125	ps
L_{ACC}	SRC Long Term Accuracy	Measured at 0V differential	–	100	ppm
T_R / T_F	SRC Rising/Falling Slew Rate	Measured differentially from ±150 mV	2.5	8	V/ns
T_{RFM}	Rise/Fall Matching	Measured single-endedly from ±75 mV	–	20	%
V_{HIGH}	Voltage High			1.15	V
V_{LOW}	Voltage Low		–0.3	–	V
V_{OX}	Crossing Point Voltage at 0.7V Swing		300	550	mV
DOT96 at 0.7V					
T_{DC}	DOT96 Duty Cycle	Measured at 0V differential	45	55	%
T_{PERIOD}	DOT96 Period	Measured at 0V differential at 0.1s	10.4156	10.4177	ns
$T_{PERIODAbs}$	DOT96 Absolute Period	Measured at 0V differential at 0.1s	10.1656	10.6677	ns
T_{CCJ}	DOT96 Cycle to Cycle Jitter	Measured at 0V differential at 1 clock	–	250	ps
L_{ACC}	DOT96 Long Term Accuracy	Measured at 0V differential at 1 clock	–	100	ppm
T_R / T_F	DOT96 Rising/Falling Slew Rate	Measured differentially from ±150 mV	2.5	8	V/ns
T_{RFM}	Rise/Fall Matching	Measured single-endedly from ±75 mV	–	20	%
V_{HIGH}	Voltage High			1.15	V
V_{LOW}	Voltage Low		–0.3	–	V
V_{OX}	Crossing Point Voltage at 0.7V Swing		300	550	mV
LCD_100_SSC at 0.7V					
T_{DC}	LCD_100 Duty Cycle	Measured at 0V differential	45	55	%
T_{PERIOD}	100 MHz LCD_100 Period	Measured at 0V differential at 0.1s	9.99900	10.0010	ns
$T_{PERIODSS}$	100 MHz LCD_100 Period, SSC -0.5%	Measured at 0V differential at 0.1s	10.02406	10.02607	ns
$T_{PERIODAbs}$	100 MHz LCD_100 Absolute Period	Measured at 0V differential at 1 clock	9.74900	10.25100	ns
$T_{PERIODSSAbs}$	100 MHz LCD_100 Absolute Period, SSC	Measured at 0V differential at 1 clock	9.74906	10.3012	ns

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
T_{CCJ}	LCD_100 Cycle to Cycle Jitter	Measured at 0V differential	–	250	ps
L_{ACC}	LCD_100 Long Term Accuracy	Measured at 0V differential	–	100	ppm
T_R / T_F	LCD_100 Rising/Falling Slew Rate	Measured differentially from ±150 mV	2.5	8	V/ns
T_{RFM}	Rise/Fall Matching	Measured single-endedly from ±75 mV	–	20	%
V_{HIGH}	Voltage High			1.15	V
V_{LOW}	Voltage Low		–0.3	–	V
V_{OX}	Crossing Point Voltage at 0.7V Swing		300	550	mV
PCI/PCIF at 3.3V					
T_{DC}	PCI Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Spread Disabled PCIF/PCI Period	Measurement at 1.5V	29.99700	30.00300	ns
$T_{PERIODSS}$	Spread Enabled PCIF/PCI Period	Measurement at 1.5V	30.08421	30.23459	ns
$T_{PERIODAbs}$	Spread Disabled PCIF/PCI Period	Measurement at 1.5V	29.49700	30.50300	ns
$T_{PERIODSSAbs}$	Spread Enabled PCIF/PCI Period	Measurement at 1.5V	29.56617	30.58421	ns
T_{HIGH}	Spread Enabled PCIF and PCI high time	Measurement at 2V	12.27095	16.27995	ns
T_{LOW}	Spread Enabled PCIF and PCI low time	Measurement at 0.8V	11.87095	16.07995	ns
T_{HIGH}	Spread Disabled PCIF and PCI high time	Measurement at 2.V	12.27365	16.27665	ns
T_{LOW}	Spread Disabled PCIF and PCI low time	Measurement at 0.8V	11.87365	16.07665	ns
T_R / T_F	PCIF/PCI Rising/Falling Slew Rate	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T_{SKEW}	Any PCI clock to Any PCI clock Skew	Measurement at 1.5V	–	1000	ps
T_{CCJ}	PCIF and PCI Cycle to Cycle Jitter	Measurement at 1.5V	–	500	ps
L_{ACC}	PCIF/PCI Long Term Accuracy	Measurement at 1.5V	–	100	ppm
48_M at 3.3V					
T_{DC}	Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Period	Measurement at 1.5V	20.83125	20.83542	ns
$T_{PERIODAbs}$	Absolute Period	Measurement at 1.5V	20.48125	21.18542	ns
T_{HIGH}	48_M High time	Measurement at 2V	8.216563	11.15198	ns
T_{LOW}	48_M Low time	Measurement at 0.8V	7.816563	10.95198	ns
T_R / T_F	Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0	2.0	V/ns
T_{CCJ}	Cycle to Cycle Jitter	Measurement at 1.5V	–	350	ps
L_{ACC}	48M Long Term Accuracy	Measurement at 1.5V	–	100	ppm
27M_NSS/27M_SS at 3.3V					
T_{DC}	Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Spread Disabled 27M Period	Measurement at 1.5V	37.03594	37.03813	ns
	Spread Enabled 27M Period	Measurement at 1.5V	37.01299	37.13172	ns
T_R / T_F	Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T_{CCJ}	Cycle to Cycle Jitter	Measurement at 1.5V	–	250	ps
L_{ACC}	27_M Long Term Accuracy	Measured at crossing point V_{OX}	–	50	ppm
REF					
T_{DC}	REF Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	REF Period	**Measurement at 1.5V**	69.82033	69.86224	ns
$T_{PERIODAbs}$	REF Absolute Period	**Measurement at 1.5V**	68.83429	70.84826	ns
T_{HIGH}	REF High time	**Measurement at 2V**	29.97543	38.46654	ns
T_{LOW}	REF Low time	**Measurement at 0.8V**	29.57543	38.26654	ns

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
T_R / T_F	REF Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	**1.0**	**4.0**	V/ns
T_{SKEW}	REF Clock to REF Clock	Measurement at 1.5V	**–**	**500**	ps
T_{CCJ}	REF Cycle to Cycle Jitter	Measurement at 1.5V	**–**	**1000**	ps
L_{ACC}	Long Term Accuracy	Measurement at 1.5V	**–**	**100**	ppm
ENABLE/DISABLE and SET-UP					
T_{STABLE}	Clock Stabilization from Power-up		**–**	**1.8**	ms
T_{SS}	Stopclock Set-up Time		**10.0**	**–**	ns

Test and Measurement Set-up

For PCI Single-ended Signals and Reference

The following diagram shows the test load configurations for the single-ended PCI, USB, and REF output signals.
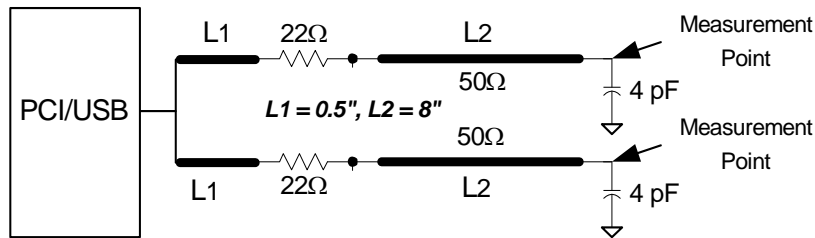
Figure 10. Single-ended PCI and USB Double Load Configuration
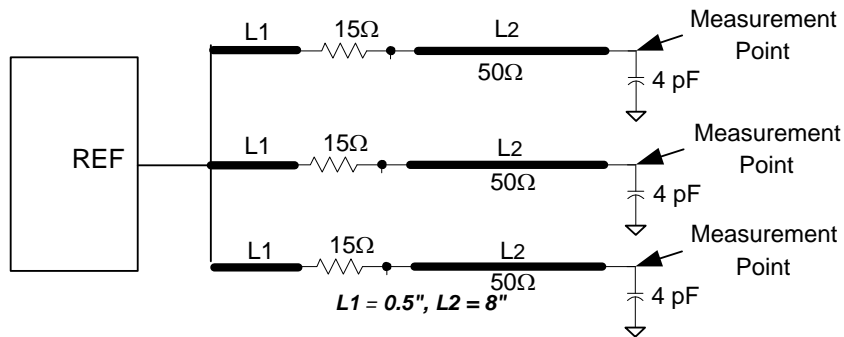
Figure 11. Single-ended REF Triple Load Configuration
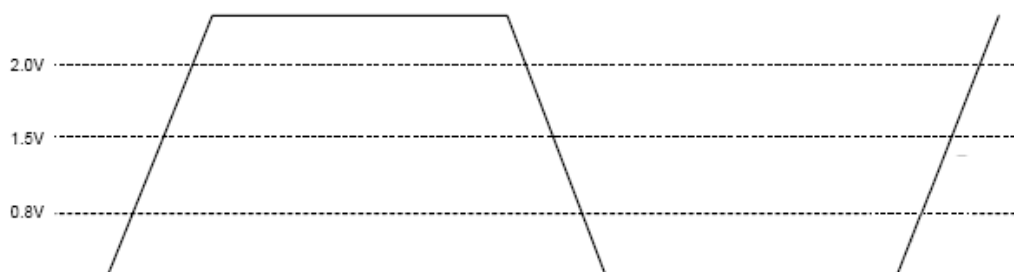
Figure 12. Single-ended Output Signals (for AC Parameters Measurement)

For CPU, SRC, and DOT96 Signals and Reference

This diagram shows the test load configuration for the differential CPU and SRC outputs
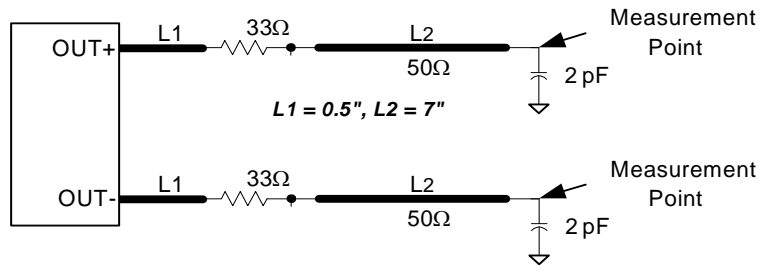
Figure 13. 0.7V Differential Load Configuration
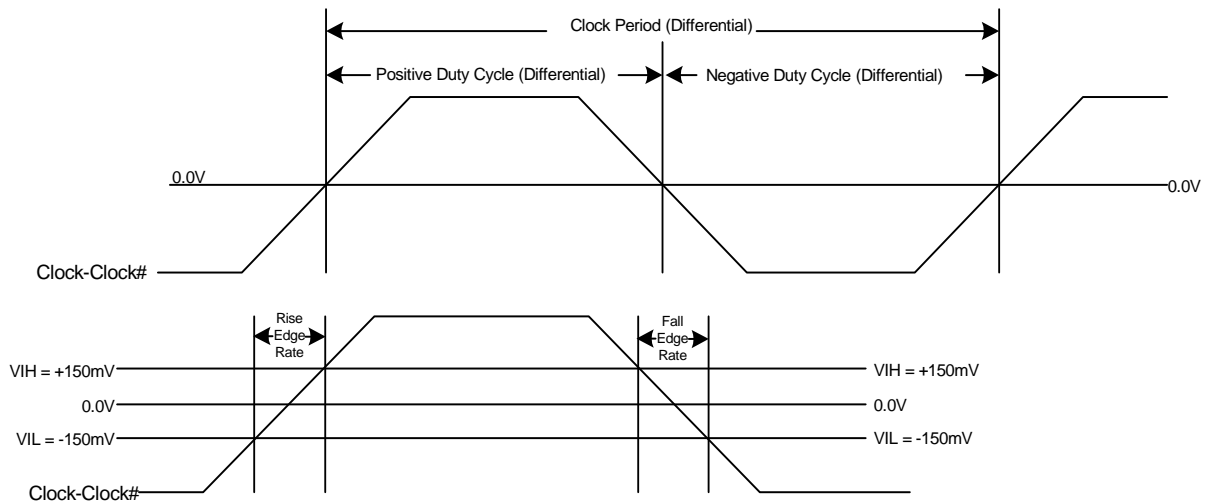
Figure 14. Differential Measurement for Differential Output Signals (for AC Parameters Measurement)
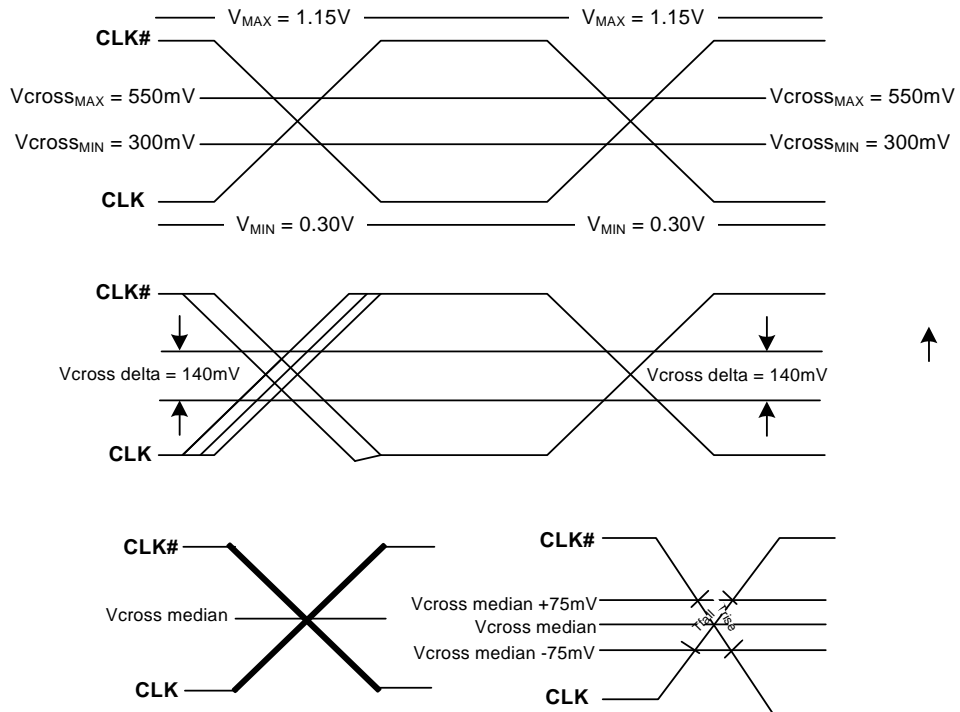
Figure 15. Single-ended Measurement for Differential Output Signals (for AC Parameters Measurement)

Ordering Information

Part Number	Package Type	Product Flow
Lead-free		
SL28506BZC	64-pin TSSOP	Commercial, 0° to 85°C
SL28506BZCT	64-pin TSSOP–Tape and Reel	Commercial, 0° to 85°C
SL28506BZI	64-pin TSSOP	Industrial, -40° to 85°C
SL28506BZIT	64-pin TSSOP–Tape and Reel	Industrial, -40° to 85°C

This device is Pb-free, Halogen-free and RoHS compliant. Parts supporting extended temperature is available upon request

Package Diagrams

64-Lead Thin Shrunk Small Outline Package (6 mm x 17 mm)
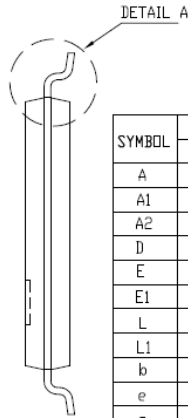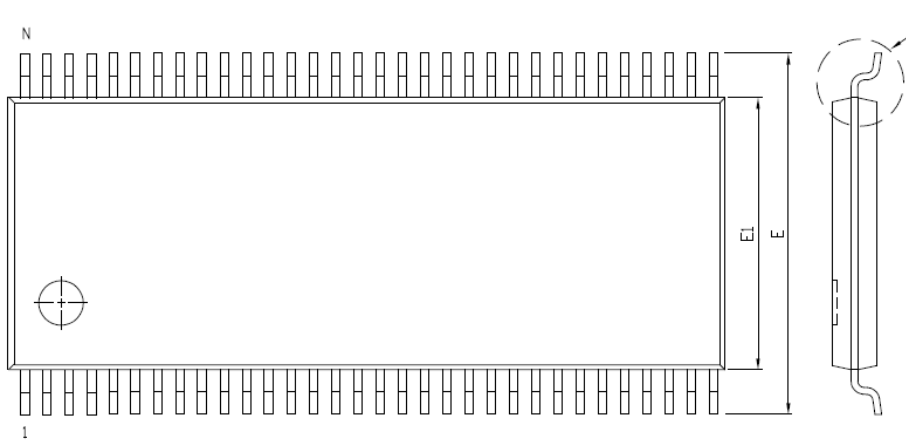
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.20			.047
A1	0.05		0.15	.002		.006
A2	0.80	1.00	1.05	.031	.039	.041
D	16.90	17.00	17.10	.665	.669	.673
E	8.00	8.10	8.20	.315	.319	.323
E1	6.00	6.10	6.20	.236	.240	.244
L	0.45	0.60	0.75	.018	.024	.030
L1	1.00 REF.			.039 REF.		
b	0.18		0.28	.007		.011
e	0.50 BSC.			.020 BSC.		
c	0.09		0.20	.004		.008
θ	0		8	0		8
N	64					
REF	JEDEC MO-153 VARIATION EF					
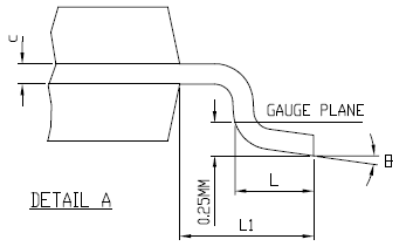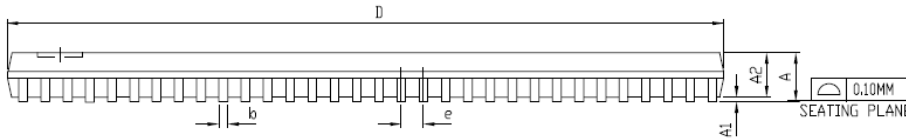
Document History Page

Document Title: SL28506 Clock Generator for Intel® Eaglelake Chipset DOC #: SP-AP-0021 (Rev AA)				
REV.	ECR#	Issue Date	Orig. of Change	Description of Change
1.0		7/12/07	JMA	New datasheet
1.1		10/30/07	JMA	1. Changed -1% spread to -0.45% spread in Byte 13 Bit 5 2. Added part number ordering information 3. Updated ordering number as general type
1.2		12/15/07	BSHEN	1. Changed Revision ID as 0001 2. Updated ordering number as SL28506BZC
1.3		8/4/08	JMA	1. Changed operating temperature range from 0C-85C to 0C-70C 2. Added note on RoHS and Pb-free 3. Removed Preliminary wording
1.4		4/1/09	JMA	1 Update Package diagram
AA	1460	4/2/10	JMA	1. Added new feature for XIN to support also CLKIN input 2. Updated revision and ordering information 3. Updated JEDEC information 4. Updated format to be ISO compliant 5. Updated commercial temperature grade back to 0C-85C 6. Merged commercial and industrial temperature 7. Added Bit 0 in Byte 3 8. Updated package ID in Byte 8 to reflect package 9. Updated Feature portion to include exclusion of SRC0 and SRC1 from PCIe Gen 2 requirements 10. Updated Byte 11 Bit 1 to be a read only bit

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