PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPD-PWR/13/8091
Dated 30 Sep 2013

BV47, IV61, IV16 Line New Passivation Material Ang Mo Kio (Singapore)

Table 1. Change Implementation Schedule

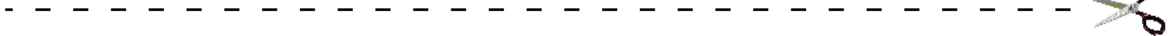
Forecasted implementation date for change	23-Sep-2013
Forecasted availability date of samples for customer	23-Sep-2013
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	23-Sep-2013
Estimated date of changed product first shipment	30-Dec-2013

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see attached list
Type of change	Waferfab process change
Reason for change	Production optimization
Description of the change	Following the continuous improvement of our service and products, this document is announcing that Power Bipolar Transistors (Planar Technology listed in this PCN), currently manufactured in Ang Mo Kio (Singapore) Wafer FAB, will be manufactured by using the yellow nitride passivation material instead of current P-VAPOX. The involved Power Bipolar Transistors (Planar Technology) produced with new passivation, guarantee the same quality and electrical characteristics as reported in the relevant data sheet. Devices used for qualification are available as samples.
Change Product Identification	By week code
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN IPD-PWR/13/8091**
Please sign and return to STMicroelectronics Sales Office	**Dated 30 Sep 2013**
☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Mottese, Anna	Marketing Manager
Aleo, Mario-Antonio	Product Manager
Falcone, Giuseppe	Q.A. Manager

Dear Customer,

Please be informed that Power Bipolar Transistors (Planar Technology listed in this PCN), currently manufactured in Ang Mo Kio (Singapore) Wafer FAB, will be manufactured by using the yellow nitride passivation material instead of current P-VAPOX.

The involved product series and affected Technologies are listed in the table below:

Product Family	Technology	Commercial Product / Series
Power Bipolar Transistors	Planar	See attached list

Any other product related to the above table, even if not expressly included or partially mentioned in the attached list, is affected by this change.

Qualification program and results availability:

The reliability test report is provided in attachment to this document.

Samples availability:

Samples of the test vehicle devices will be available on request starting from week 37-2013.
Any other sample request will be processed and scheduled by Power Transistor Division upon request.

Product Family	Package	Part Number - Test Vehicle
Power Bipolar Transistors	TO-220 TO-220FP	BUL742C BUL1102EFP

Change implementation schedule:

The first shipments will be implemented according to our work in progress and materials availability:

Product Family	1st Shipments
Power Bipolar Transistors	From Week 50-2013

Marking and traceability:

Unless otherwise stated by customer specific requirement, traceability of Power Bipolar Transistors (Planar Technology), manufactured using the yellow nitride passivation, will be ensured by week code.

Sincerely Yours.

P-VAPOX Vs. YELLOW NITRIDE

Contents

1. Parametric Verification on:

- **BVCEO;**
- **Iceo, Ices**
- **hfe;**
- **VCEsat;**

2. CPKs data.

LEGEND:

- P-VAPOX distribution on the left,
- YELLOW NITRIDE distribution on the right.

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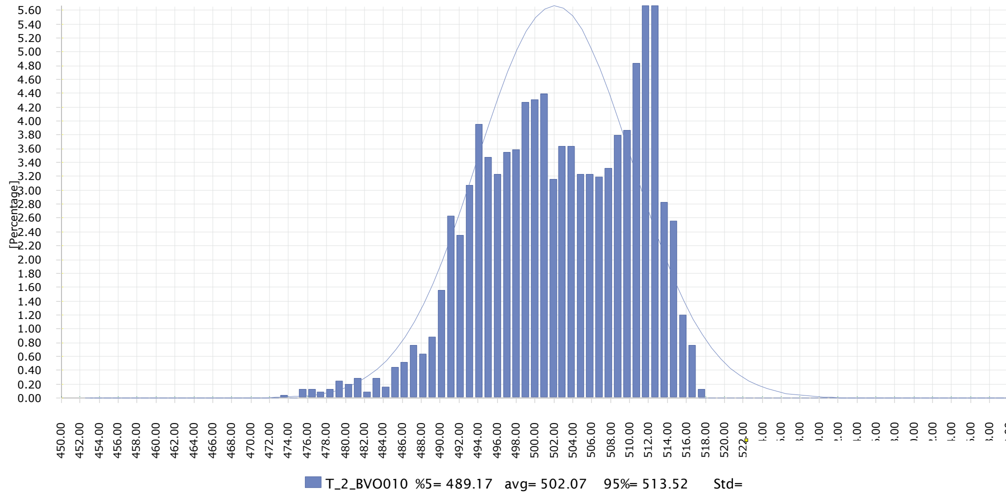
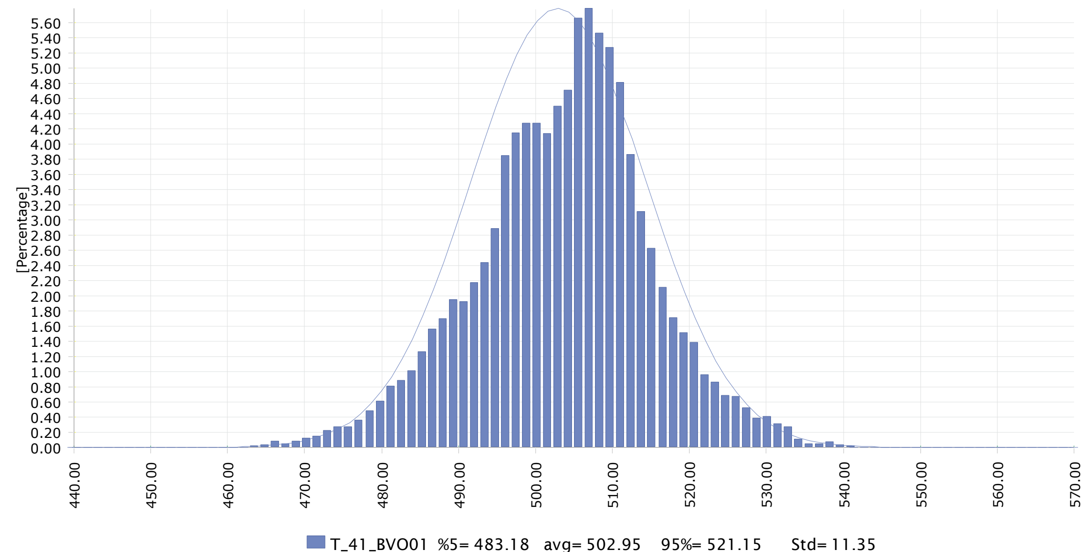
P-VAPOX Vs. YELLOW NITRIDE

PARAMETRIC VERIFICATION BVceo @ 100mA





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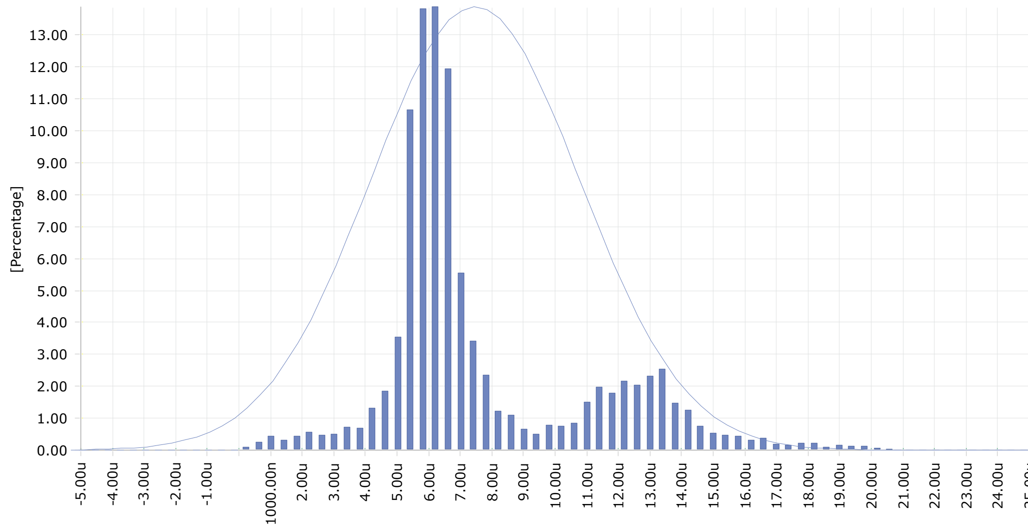
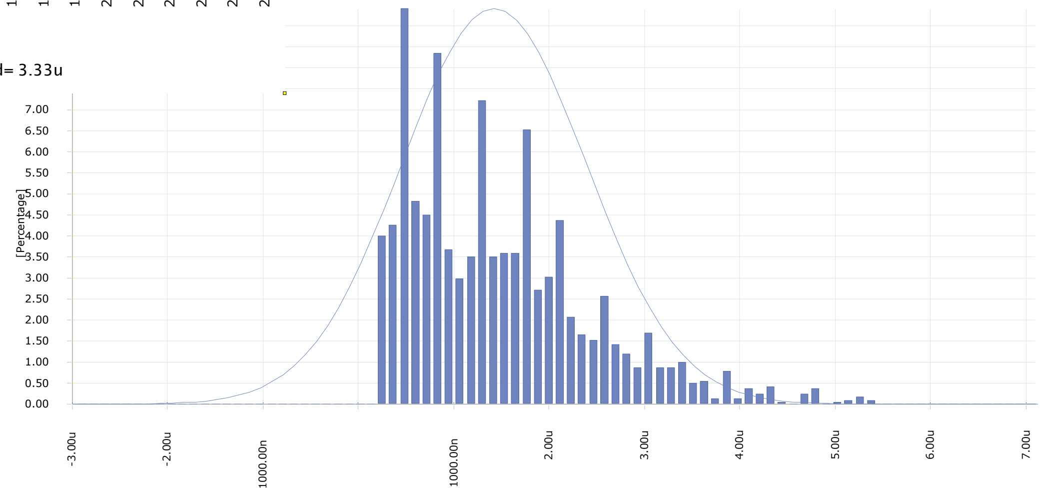
P-VAPOX Vs. YELLOW NITRIDE

PARAMETRIC VERIFICATION Iceo @ 450V





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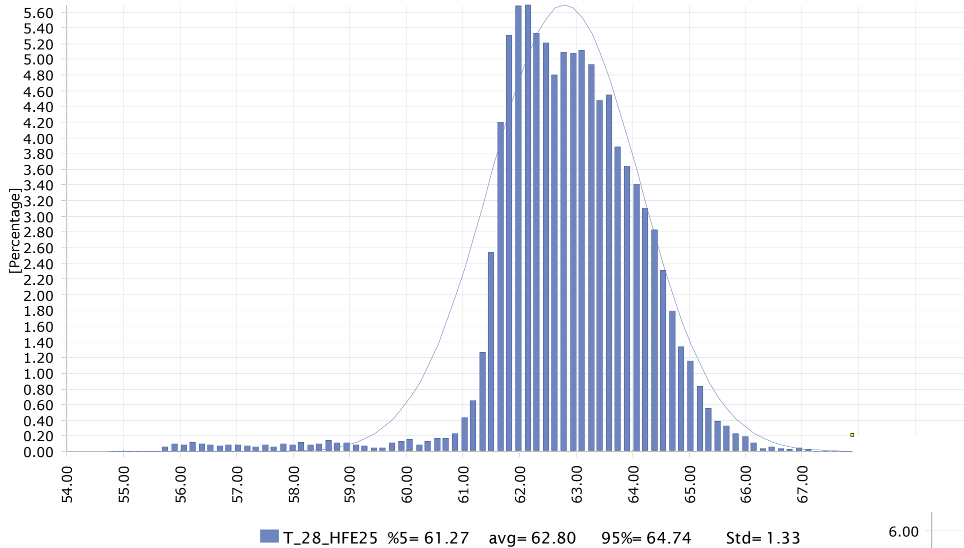
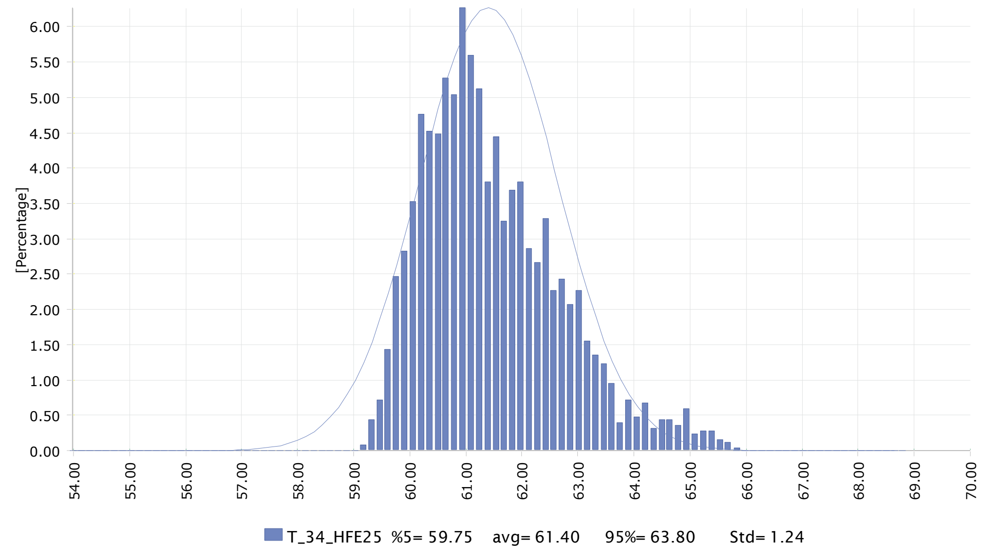
P-VAPOX Vs. YELLOW NITRIDE

PARAMETRIC VERIFICATION hfe @ 5V 250mA





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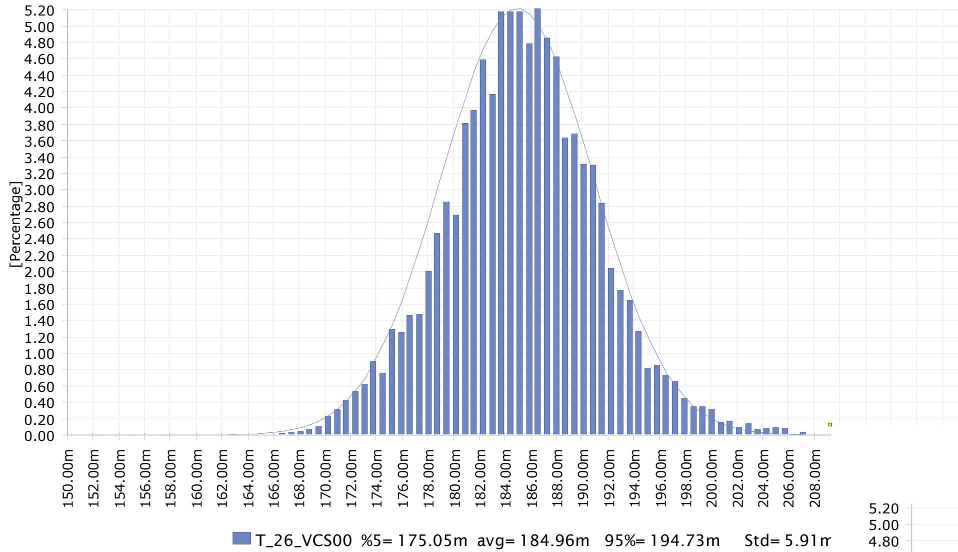
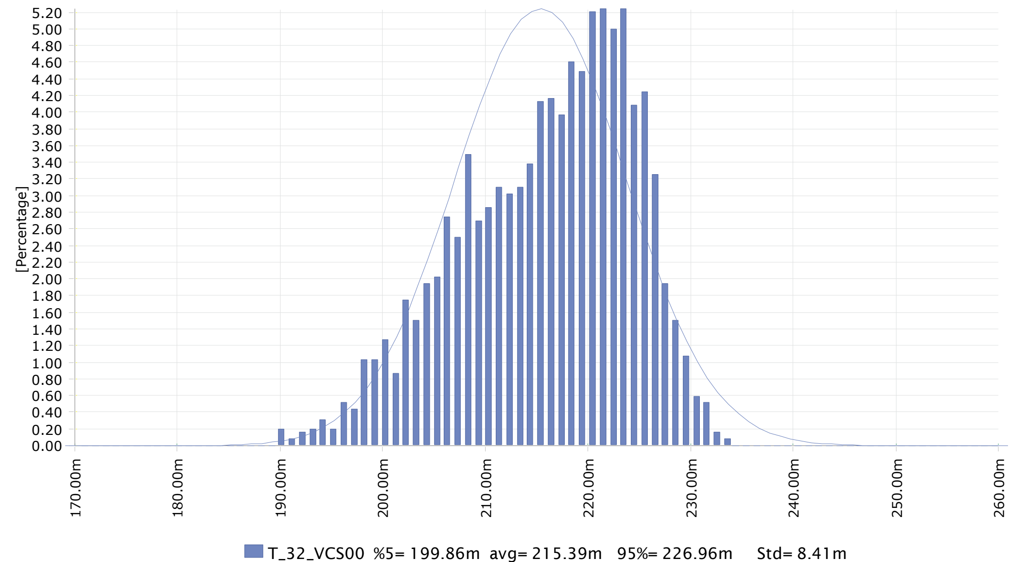
P-VAPOX Vs. YELLOW NITRIDE

PARAMETRIC VERIFICATION VCEsat @ 2A 400mA





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P-VAPOX Vs. YELLOW NITRIDE

Limits (min & max) and CPK

Limits (min & max) and CPK

Commercial Product: **BUL1102E / BUL1102EFP**

PROCESS:		**P-VAPOX**		**YELLOW NITRIDE**
Test name	Bvceo @ 100mA			
	min:	450V	min:	450V
	max:		max:	
	CPK	**2.12**	CPK	**1.55**
Test name	Iceo @ 450V			
	min:		min:	
	max:	100µA	max:	100µA
	CPK	**9.26**	CPK	**33.84**
Test name	hfe @ 5V 0.25A			
	min:	35	min:	35
	max:	70	max:	70
	CPK	**1.80**	CPK	**2.31**
Test name	VCEsat @ 2A 0.4A			
	min:		min:	
	max:	1.5V	max:	1.5V
	CPK	**74.17**	CPK	**50.91**

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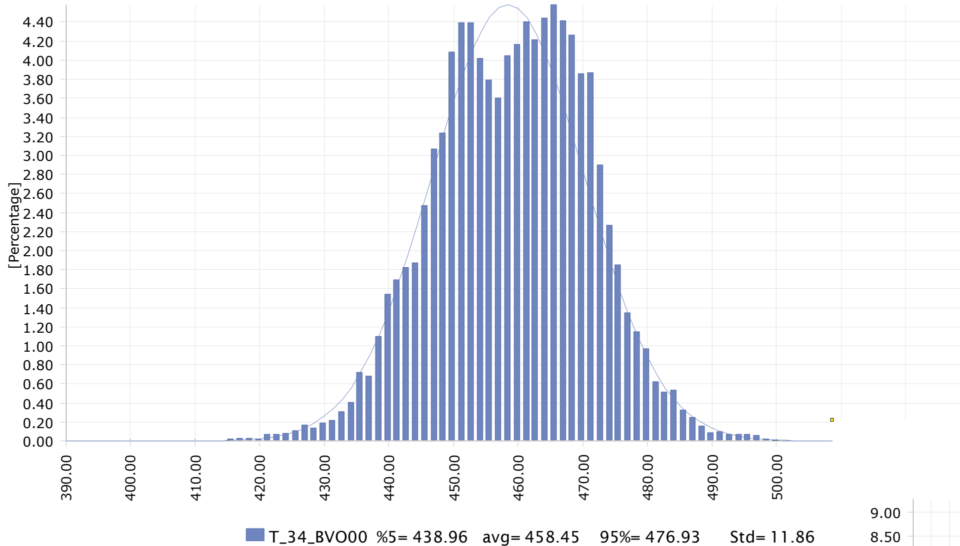
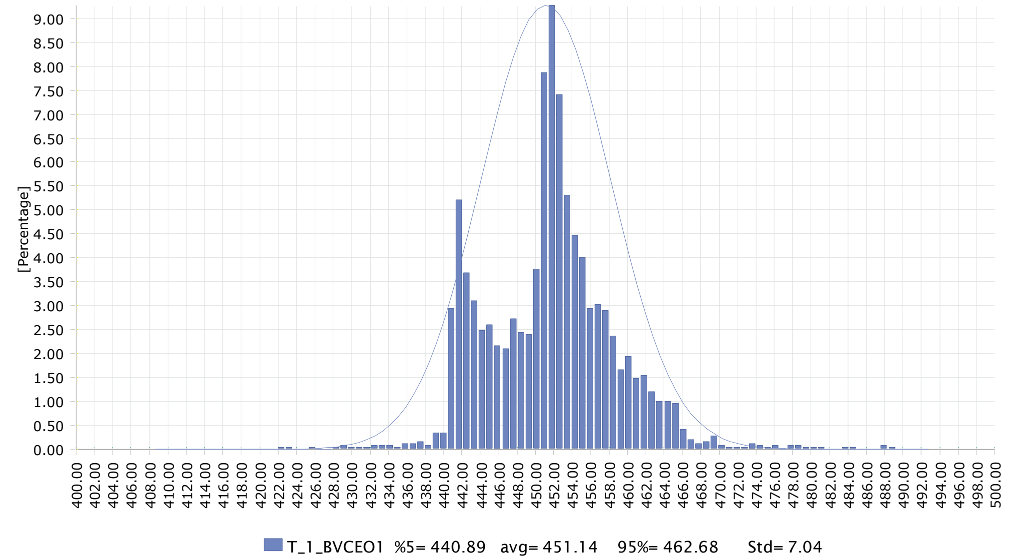
P-VAPOX Vs. YELLOW NITRIDE

PARAMETRIC VERIFICATION BVceo @ 100mA

BUL742C / BULD742CT4
BVCEO @ 10mA P-VAPOX



BUL742C / BULD742CT4
BVCEO @ 10mA YELLOW NITRIDE



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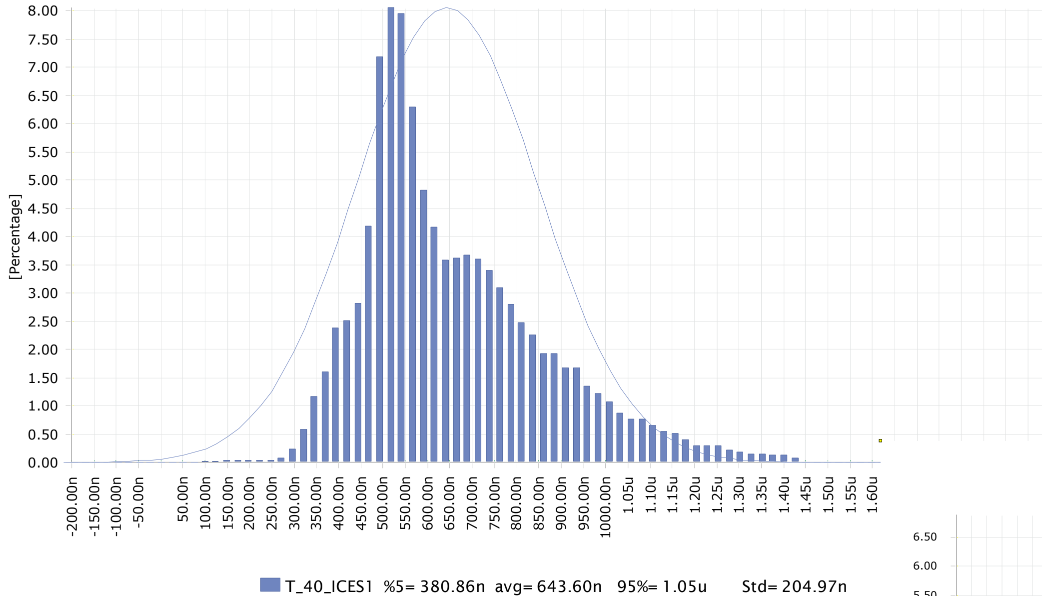
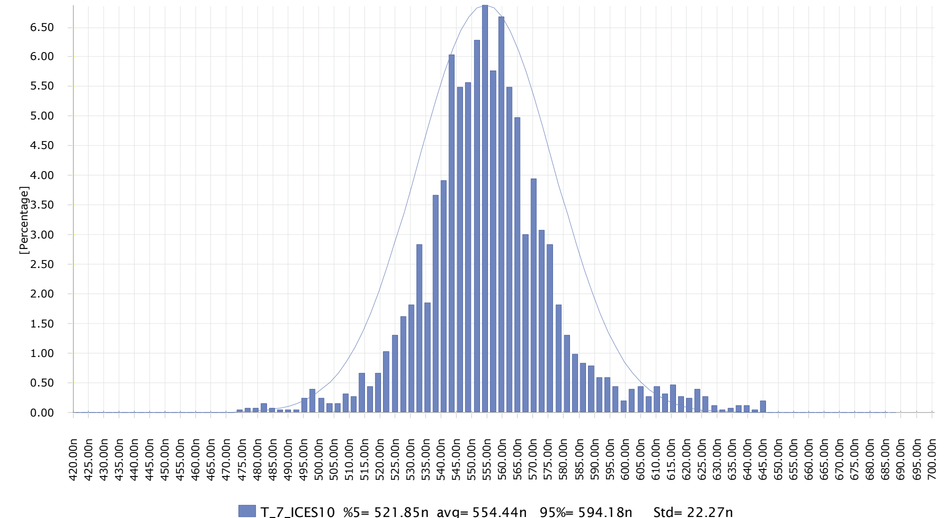
P-VAPOX Vs. YELLOW NITRIDE

PARAMETRIC VERIFICATION Ices @ 1070V





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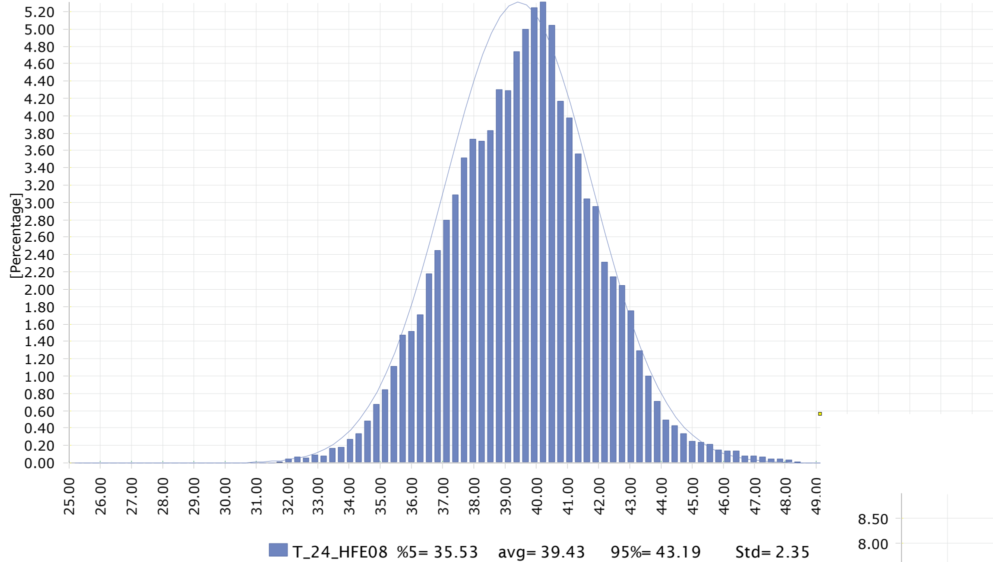
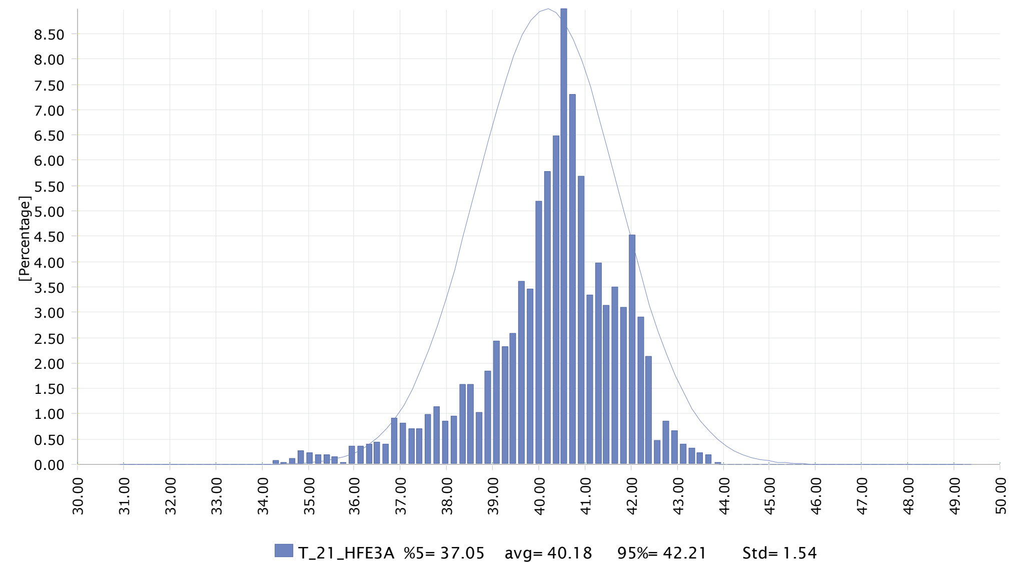
P-VAPOX Vs. YELLOW NITRIDE

PARAMETRIC VERIFICATION hfe @ 3V 800mA





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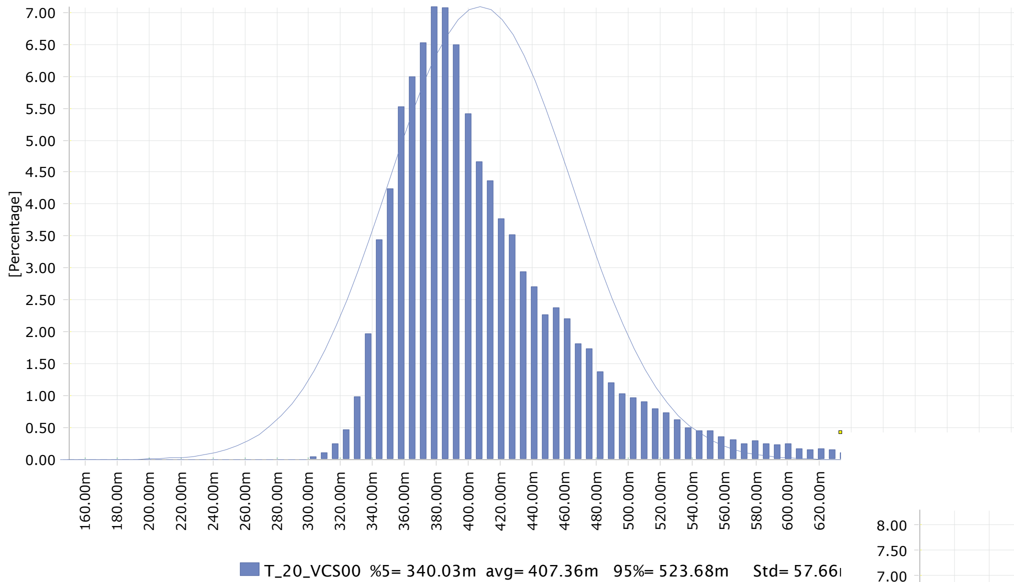
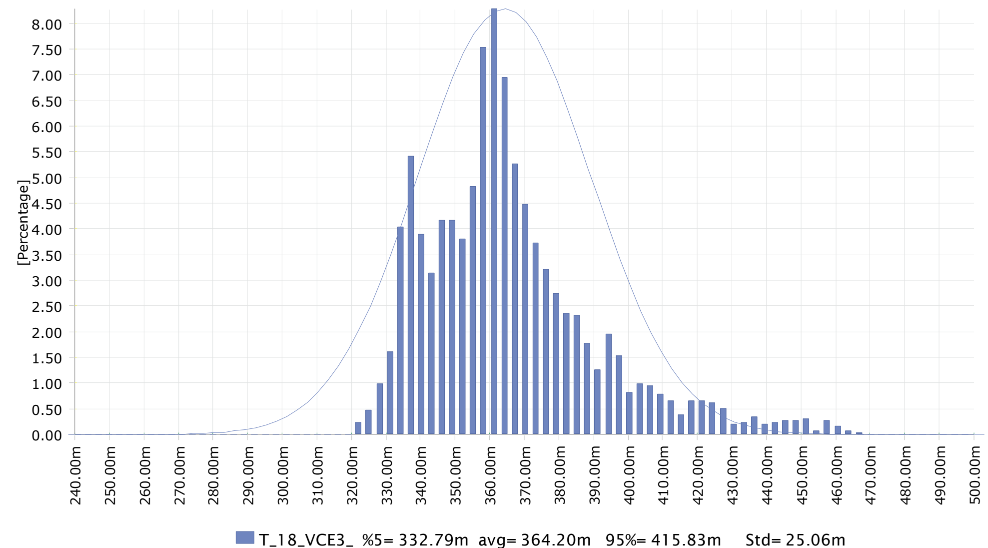
P-VAPOX Vs. YELLOW NITRIDE

PARAMETRIC VERIFICATION VCEsat @ 3.5A 1A





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P-VAPOX Vs. YELLOW NITRIDE

Limits (min & max) and CPK

Limits (min & max) and CPK

Commercial Product: **BUL742C / BULD742CT4**

PROCESS:	**P-VAPOX**		**YELLOW NITRIDE**	
Test name	Bvceo @ 10mA			
	min:	400V	min:	400V
	max:		max:	
	CPK	**1.64**	CPK	**2.42**
Test name	Ices @ 1070V			
	min:		min:	
	max:	10µA	max:	10µA
	CPK	**15.28**	CPK	**141.38**
Test name	hfe @ 3V 0.8A			
	min:	25	min:	25
	max:	50	max:	50
	CPK	**1.49**	CPK	**2.12**
Test name	VCEsat @ 3.5A 1A			
	min:		min:	
	max:	1.5V	max:	1.5V
	CPK	**6.31**	CPK	**15.10**

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Reliability Report

BV47, IV61, IV16 Line New Passivation Material
Ang Mo Kio (Singapore)

General Information	
Product Test Vehicles Lines:	BV47 / IV61
Product Families:	Power Bipolar Transistors
P/Ns:	BUL1102EFP (BV47) BUL1102E (BV47) BUL741FP (IV61) BUL741 (IV61)
Product Group:	IMS – IPG
Product division:	Power Transistor Division
Package:	TO-220 / TO-220FP
Silicon Process techn.:	High voltage fast switching PLANAR Power Bipolar

Locations	
Wafer Diffusion Plants:	*Ang Mo Kio (Singapore)*
EWS Plants:	*Ang Mo Kio (Singapore)*
Assembly plant:	*ST Longgang (China)*
Reliability Lab:	*IMS-IPG Catania Reliability Lab.*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	September 2013	9	C. Cappello	G.Falcone	First issue

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size
HF	Halogen Free

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Qualification of new YELLOW NITRIDE passivation material instead of current P-VAPOX one for Power Bipolar Transistors (Planar Technology), currently manufactured in Ang Mo Kio (Singapore) Wafer FAB.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

PLANAR Power Bipolar.

4.2 Construction note

D.U.T.: BUL1102EFP LINE: BV47 PACKAGE: TO-220FP

Wafer/Die fab. information	
Wafer fab manufacturing location	*Ang Mo Kio (Singapore)*
Technology	PLANAR Power Bipolar
Die finishing back side	Ti/Ni/Ag
Die size	2430 x 2460 μm^2
Metal	Al/Si
Passivation type	Yellow Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	*Ang Mo Kio (Singapore)*
Test program	WPIS

Assembly information	
Assembly site	ST Longgang (China)
Package description	TO-220FP
Molding compound	HF Epoxy Resin
Frame material	Cu selected Ni/NiP
Die attach process	Soft solder (Pb/Sn/Ag)
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg 5 mils
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	ST Longgang (China)
Tester	LTX IPTESTER

D.U.T.: BUL1102E LINE: BV47 PACKAGE: TO-220

Wafer/Die fab. information	
Wafer fab manufacturing location	*Ang Mo Kio (Singapore)*
Technology	PLANAR Power Bipolar
Die finishing back side	Ti/Ni/Ag
Die size	2430 x 2460 μm^2
Metal	Al/Si
Passivation type	Yellow Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	*Ang Mo Kio (Singapore)*
Test program	WPIS

Assembly information	
Assembly site	ST Longgang (China)
Package description	TO-220
Molding compound	HF Epoxy Resin
Frame material	Cu selected Ni/NiP
Die attach process	Soft solder (Pb/Sn/Ag)
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg 5 mils
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	ST Longgang (China)
Tester	LTX IPTESTER

D.U.T.: BUL741FP LINE: IV61 PACKAGE: TO-220FP

Wafer/Die fab. information	
Wafer fab manufacturing location	*Ang Mo Kio (Singapore)*
Technology	PLANAR Power Bipolar
Die finishing back side	Ti/Ni/Ag
Die size	2430 x 2460 μm^2
Metal	Al/Si
Passivation type	Yellow Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	*Ang Mo Kio (Singapore)*
Test program	WPIS

Assembly information	
Assembly site	ST Longgang (China)
Package description	TO-220FP
Molding compound	HF Epoxy Resin
Frame material	Cu selected Ni/NiP
Die attach process	Soft solder (Pb/Sn/Ag)
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg 5 mils
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	ST Longgang (China)
Tester	LTX IPTESTER

D.U.T.: BUL741 LINE: IV61 PACKAGE: TO-220

Wafer/Die fab. information	
Wafer fab manufacturing location	*Ang Mo Kio (Singapore)*
Technology	PLANAR Power Bipolar
Die finishing back side	Ti/Ni/Ag
Die size	2430 x 2460 μm^2
Metal	Al/Si
Passivation type	Yellow Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	*Ang Mo Kio (Singapore)*
Test program	WPIS

Assembly information	
Assembly site	ST Longgang (China)
Package description	TO-220
Molding compound	HF Epoxy Resin
Frame material	Cu selected Ni/NiP
Die attach process	Soft solder (Pb/Sn/Ag)
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg 5 mils
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	ST Longgang (China)
Tester	LTX IPTESTER

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	BUL1102EFP	BV47	Power BIPOLAR
2	BUL1102E	BV47	Power BIPOLAR
3	BUL741FP	IV61	Power BIPOLAR
4	BUL741	IV61	Power BIPOLAR

5.2 Reliability test plan summary

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS				Note
						LOT1	LOT2	LOT3	LOT4	
Die Oriented Tests										
HTRB	N	JESD22 A-108	TA = 150°C, BIAS=880V (BV47) BIAS=840V (IV61)	77 x 4 lots	168 H	0/77	0/77	0/77	0/77	
					500 H	0/77	0/77	0/77	0/77	
					1000 H	0/77	0/77	0/77	0/77	
HTSL	N	JESD22 A-103	TA = 150°C	77 x 4 lots	168 H	0/77	0/77	0/77	0/77	
					500 H	0/77	0/77	0/77	0/77	
					1000 H	0/77	0/77	0/77	0/77	
Package Oriented Tests										
AC	N	JESD22 A-102	Pa=2Atm / TA=121°C	77 x 4 lots	96 H	0/77	0/77	0/77	0/77	
TC	N	JESD22 A-104	TA = -65°C to 150°C	77 x 4 lots	100 cy	0/77	0/77	0/77	0/77	
					200 cy	0/77	0/77	0/77	0/77	
					500 cy	0/77	0/77	0/77	0/77	
TF/IOL	N	Mil-Std 750D Method 1037	ΔTC=105°C	20 x 4 lots	10Kcy	0/20	0/20	0/20	0/20	
H3TRB	N	JESD22 A-101	TA=85°C , RH=85% , BIAS=100V	77 x 4 lots	168 H	0/77	0/77	0/77	0/77	
					500 H	0/77	0/77	0/77	0/77	
					1000 H	0/77	0/77	0/77	0/77	

6 ANNEXES 6.0

6.1Tests Description

Test name	Description	Purpose
Die Oriented		
HTRB High Temperature Reverse Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
AC Auto Clave	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
TF / IOL Thermal Fatigue / Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
H3TRB / THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

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