

# SG6516

## PC Power Supply Supervisors

### Features

- Two 12V Sense Input Pins: VS12 and VS12B
- Over-Voltage Protection (OVP) for 3.3V, 5V, and two 12V
- Over-Current Protection (OCP) for 3.3V, 5V, and two 12V
- Under-Voltage Protection (UVP) for 3.3V, 5V, and two 12V
- Open-Drain Output for PGO and FPO Pins
- 300ms Power-Good Delay
- 2.8ms PSON Control to FPO Turn-off Delay
- 48ms PSON Control Delay
- No Lock-up During the Fast AC Power On/Off
- Wide Supply Voltage Range: 4V to 15V

### Applications

- Switch-Mode Power Supplies with Active PFC
- Servo System Power Supplies
- PC-ATX Power Supplies

### Description


The SG6516 is designed to provide the supply voltage, current supervisor, remote on/off (PSON), power good (PGO) indicator, and fault protection (FPO) functions for switching power systems.

For supervisory functions, it provides the over-voltage protection (OVP) for 3.3V, 5V, and two 12V; over-current protection (OCP) for 3.3V, 5V, and two 12V; under-voltage protection (UVP) for 3.3V, 5V, and two 12V. When 3.3V, 5V, or 12V voltage decreases to 2.3V, 3.5V, and 9V, respectively, the under-voltage protection function is enabled. FPO is set HIGH to turn off the PWM controller IC. The voltage difference across external current shunt is used for OCP functions. An external resistor can be used to adjust the protection threshold. An additional protection input pin provides the flexibility for designing protection circuits.

The power supply is turned on after a 48ms delay when PSON signal is set from HIGH to LOW. To turn off the power supply, the PSON signal is set from LOW to HIGH with a delay of 48ms. The PGI circuitry provides a power-down warning signal for PGO. When PGI input is lower than the internal 1.25V reference voltage, the PGO signal is pulled LOW.

### Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
SG6516DZ	-40°C to +85°C	16-pin Dual In-Line Package (DIP)	Rail
SG6516SZ	-40°C to +85°C	16-pin Small Outline Package (SOP)	Tape & Reel

 All packages are lead free per JEDEC: J-STD-020B standard.

Application Diagram

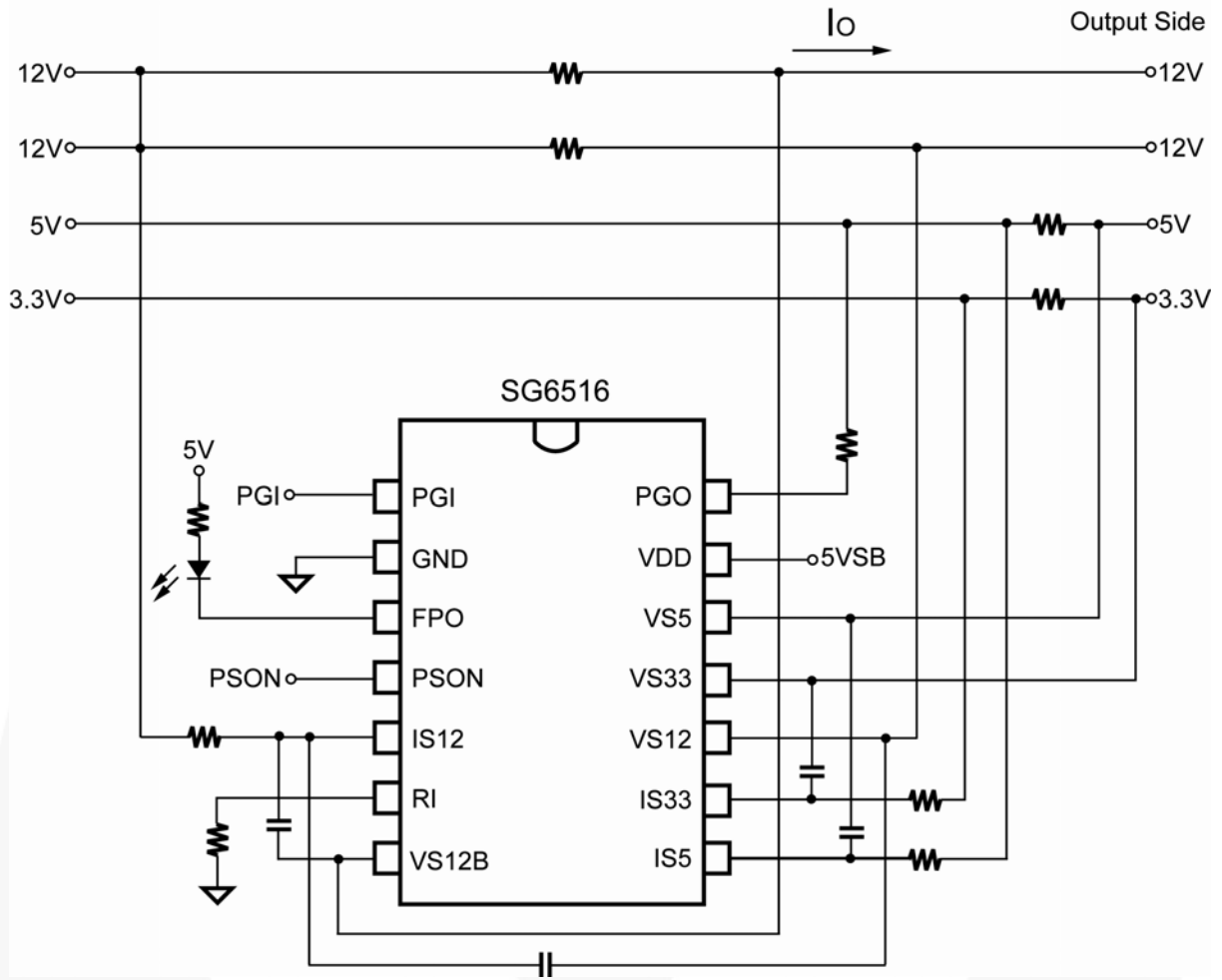


Figure 1. Typical Application

Block Diagram

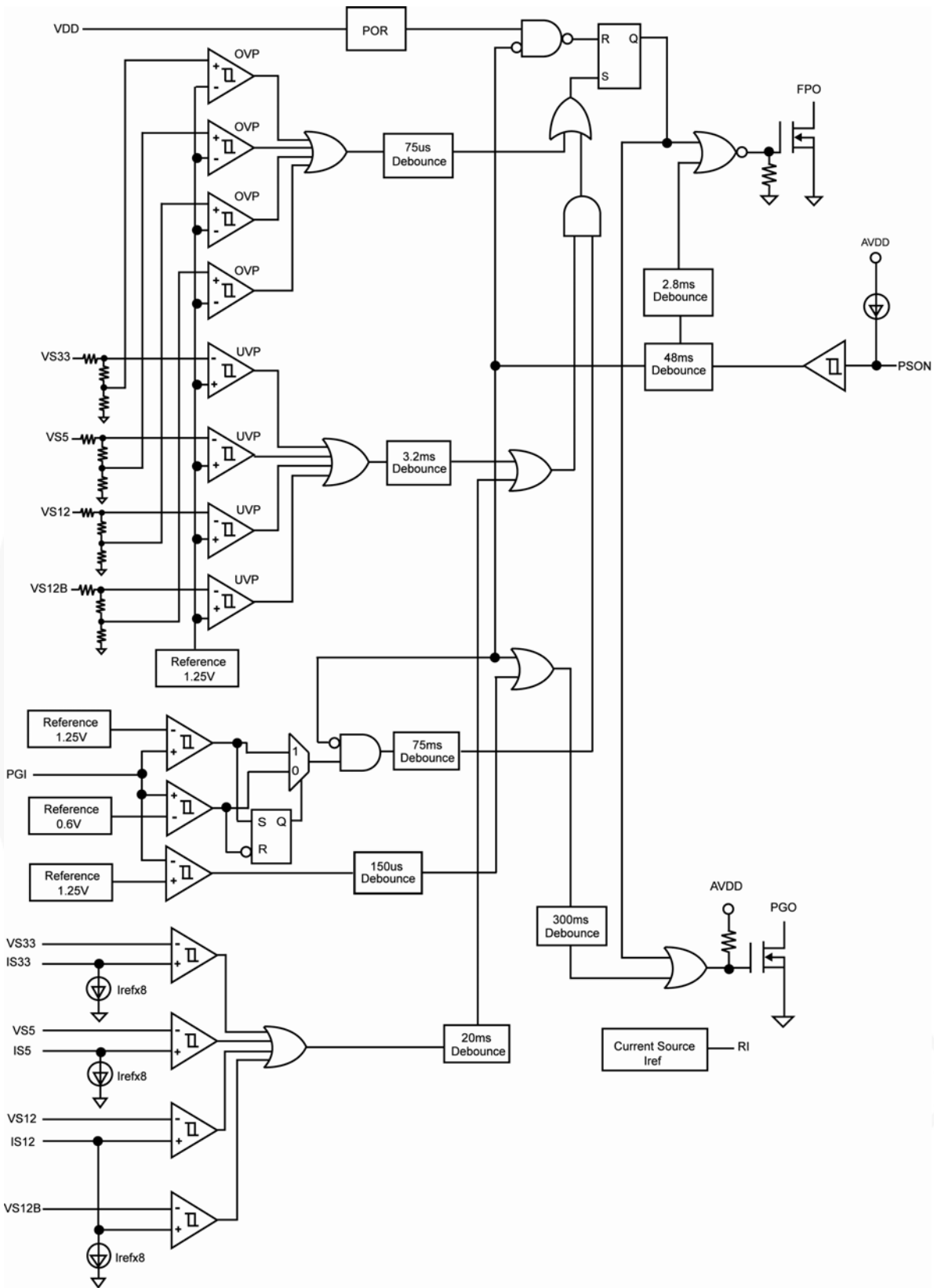


Figure 2. Function Block Diagram

## Pin Configuration

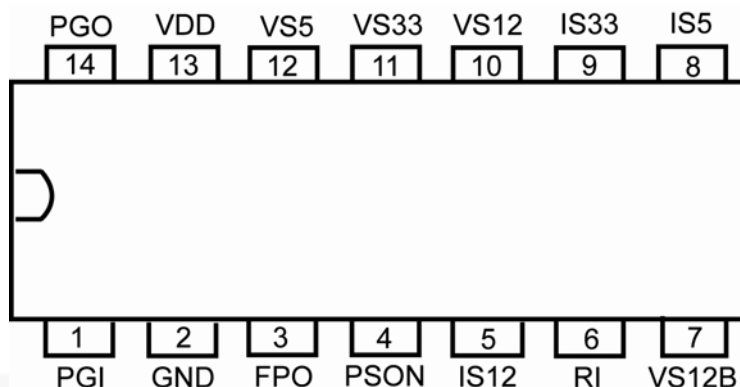


Figure 3. Pin Configuration(Top View)

## Pin Definitions

Pin #	Name	Description
1	PGI	<b>Power Good Input.</b> For ATX SMPS, it detects AC line voltage through the main transformer.
2	GND	<b>Ground.</b>
3	FPO	<b>Fault Protection Output.</b> Output signal to control the primary PWM IC through an opto-coupler. When FPO is low, the PWM IC is enabled.
4	PSON	<b>Remote on/off logic input from CPU or main board.</b> The power supply is turned on/off after a 48ms delay.
5	IS12	<b>12V over-current protection sense input.</b> For typical applications, this pin is connected to the positive end of a current shunt through one resistor. When the voltage on IS12 is higher than that of VS12 by 5mV, OCP is enabled.
6	RI	<b>Reference setting.</b> One external resistor, $R_i$ , connected between the RI and GND pins, determines a reference current, $I_{REF}=1.25/R_i$ , for OCP programming.
7	VS12B	<b>Second 12V over/under-voltage control sense input.</b>
8	IS5	<b>5V over-current protection sense input.</b>
9	IS33	<b>3.3V over-current protection sense input.</b>
10	VS12	<b>12V over/under-voltage control sense input.</b>
11	VS33	<b>3.3V over/under-voltage control sense input.</b>
12	VS5	<b>5V over/under-voltage control sense input.</b>
13	VDD	<b>Supply voltage:</b> 4.2V ~ 15V. For ATX SMPS, it is connected to 5V-standby and 12V through diodes, respectively.
14	PGO	<b>Power-Good logic Output,</b> 0 or 1 (open-drain). Power good=1 means that the power supply is good for operation. The power-good delay is 300ms.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. All voltage values, except differential voltage, are given with respect to GND pin.

Symbol	Parameter		Min.	Max.	Unit
V <sub>DD</sub>	DC Supply Voltage			16	V
V <sub>IN</sub>	Input Voltage	PSON, PGI, VS5, IS5, VS33, IS33	-0.3	7.0	V
		VS12, VS12B, IS12	-0.3	15.0	V
V <sub>OUT</sub>	Output Voltage	FPO, PGO	-0.3	8.0	V
T <sub>J</sub>	Operating Junction Temperature		-40	+125	°C
T <sub>STG</sub>	Storage Temperature Range		-55	+150	°C
T <sub>L</sub>	Lead Temperature (Soldering)			+260	°C
ESD	Electrostatic Discharge Capability, Human Body Model			3.0	KV
	Electrostatic Discharge Capability, Machine Model			200	V

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
T <sub>A</sub>	Operating Ambient Temperature	-40		+85	°C

## Electrical Characteristics

$V_{DD}=5V$ ,  $T_A=25^{\circ}C$ , unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
<b>V<sub>DD</sub> Section</b>						
V <sub>DD</sub>	DC Supply Voltage		4.2		15.0	V
I <sub>DD1</sub>	Supply Current 1	PSON=LOW		1.7	2.6	mA
I <sub>DD2</sub>	Supply Current 2	PSON=HIGH		1.0	1.5	mA
t <sub>R</sub>	Supply Voltage Rising Time		1			ms
V <sub>ST</sub>	V <sub>DD</sub> Start Threshold Voltage				4.2	V
<b>Over-Voltage (OVP) and Over-Current (OCP) Protections</b>						
V <sub>OVP</sub>	Over-Voltage Protection	VS33	3.7	3.9	4.1	V
		VS5	5.7	6.1	6.5	
		VS12, VS12B	13.2	13.8	14.4	
I <sub>REF</sub>	Ratio of Current-Sense Sink Current to Current-Sense Setting Pin (RI) Source Current	R <sub>I</sub> =18.5kΩ ~ 75kΩ	7.6	8.0	8.4	
V <sub>OFFSET</sub>	OCP Comparator Input Offset Voltage		-3		3	mV
I <sub>LKG-FPO</sub>	Leakage Current (FPO)	FPO=5V			5	μA
V <sub>OL-FPO</sub>	Low Level Output Voltage (FPO)	I <sub>SINK</sub> 20mA			0.4	V
t <sub>OVP</sub>	OVP Delay Time		33	75	110	μs
t <sub>OCP</sub>	OCP Delay Time		12.5	20.0	27.5	ms
V <sub>RI</sub>	RI Pin Voltage		0.98•Typ.	1.25	1.01•Typ.	V
I <sub>RI</sub>	Output Current RI		12.5		62.5	μA
t <sub>ST-OCP</sub>	Start-up OCP / UVP Protection Time	0.6V < PGI < 1.25V; FPO=Low	49	75	114	ms
<b>Under-Voltage Protection and PGI, PGO</b>						
V <sub>PGI_1</sub>	Input Threshold Voltage	PGI 1	0.98•Typ.	1.25	1.02•Typ.	V
V <sub>PGI_2</sub>	Input Threshold Voltage	PGI 2	0.96•Typ.	0.60	1.03•Typ.	V
V <sub>UVP</sub>	Under-Voltage Protection	VS33	2.1	2.3	2.5	V
		VS5	3.3	3.5	3.7	
		VS12, VS12B	8.5	9.0	9.5	
t <sub>OND</sub>	Under Voltage Turn-on Delay	PGI>0.6V	49	75	114	ms
t <sub>UVP</sub>	UVP Delay	PGI>1.25V	2.4	3.2	4.0	ms
I <sub>LKG-PGO</sub>	Leakage Current (PGO)	PGO=5V			5	μA
V <sub>OL-PGO</sub>	Low Level Output Voltage (PGO)	V <sub>DD</sub> =12V; I <sub>SINK</sub> 10mA			0.4	V
t <sub>PG</sub>	Timing PG Delay		200	300	450	ms
t <sub>ND1</sub>	Noise Deglitch Time		90	150	210	μs
<b>PSON Control</b>						
I <sub>PSON</sub>	Input Pull-up Current	PSON=0V		120		μA
V <sub>IH</sub>	High-level Input Voltage		2			V
V <sub>IL</sub>	Low-level Input Voltage				0.8	V
t <sub>PSON</sub>	Timing PSON to On/Off	PSON LOW to FPO LOW	34	48	67	ms
		PSON HIGH to PGO LOW	34	48	67	
t <sub>PSOFF</sub>	Timing PGO LOW to FPO HIGH		1.6	2.8	4.5	ms

## Functional Description

The SG6516 provides over-current protection for the 3.3V, 5V, and two 12V rails. Whenever an OCP condition occurs at any of the voltage rails, PGO is LOW and FPO is open. The internal OCP comparators have a very small offset voltage ( $\pm 3\text{mV}$ ). The sink currents of IS33, IS5, and IS12 are eight times the current at the RI pin. The current at the RI pin is  $V_{RI}/R_I$ .

The following example demonstrates how to set the over-current protection. If  $I_1 \times R_1 > I_{RI} \times R_2$ , OCP is active. If  $R_1=5\text{m}\Omega$ ,  $R_I=30\text{K}\Omega$ , and the OCP active level is 35A; the  $R_2$  resistor is:

$$R_2 = \frac{I_1 \times R_1}{I_{RI} \times 8} = 525\Omega \quad (1)$$

where C is bypass noise, with a suggested value between  $1\mu\text{F} \sim 2.2\mu\text{F}$

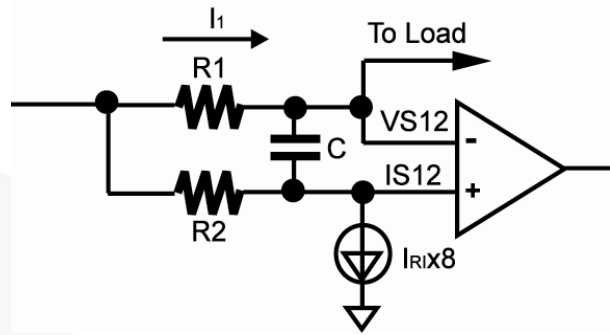


Figure 4. OCP Set-up

Timing Chart

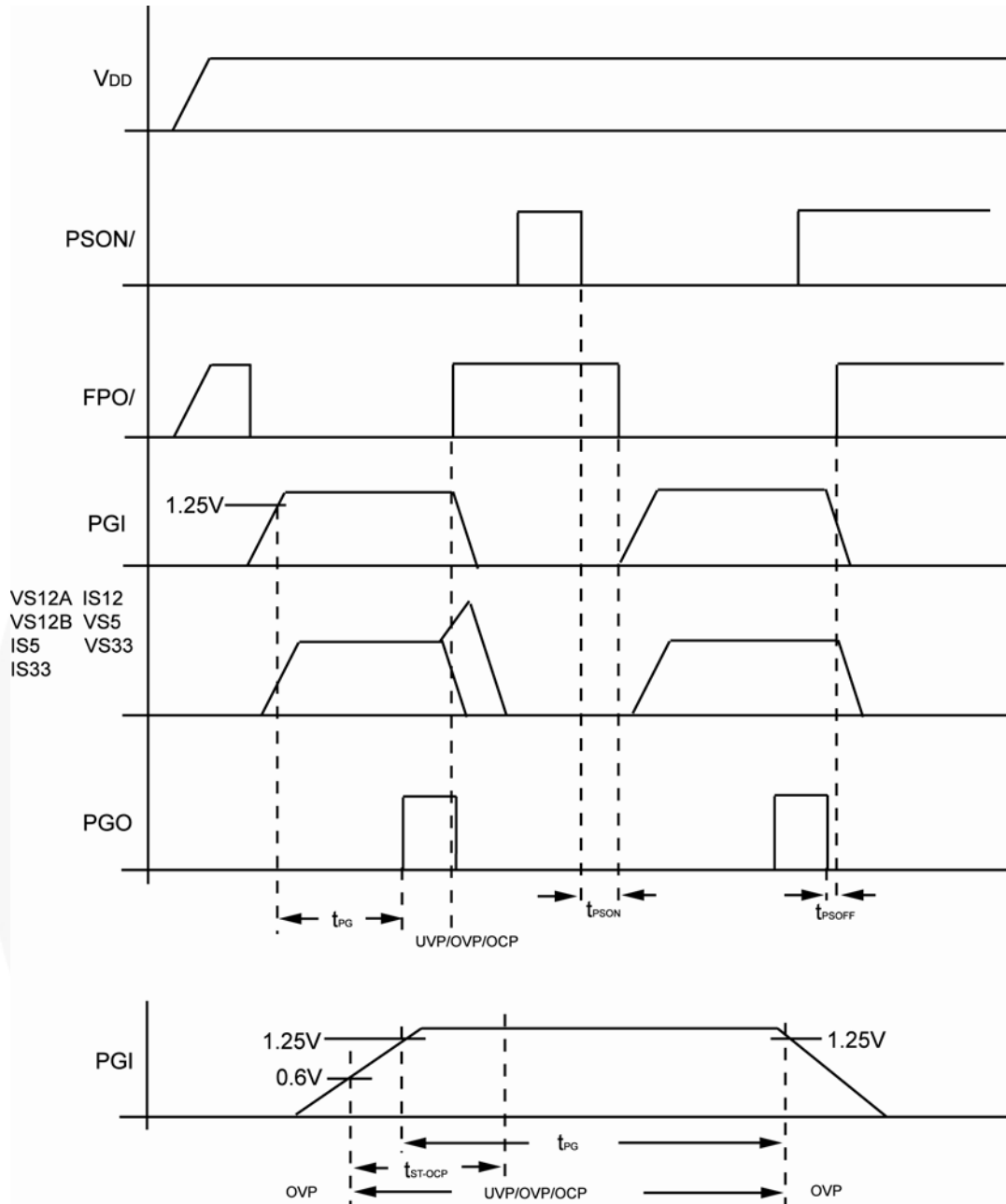


Figure 5. Timing Diagram



## Typical Performance Characteristics

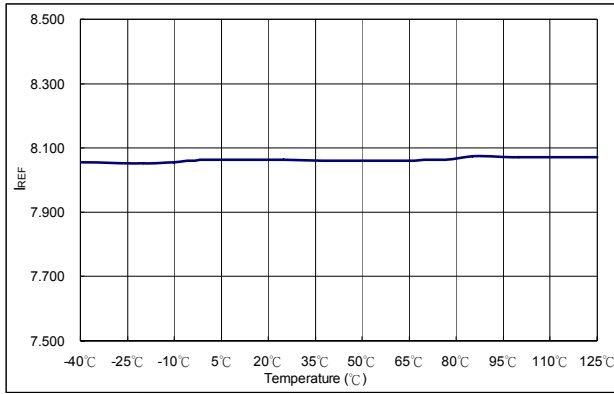


Figure 6. I<sub>REF</sub> vs. T<sub>A</sub>

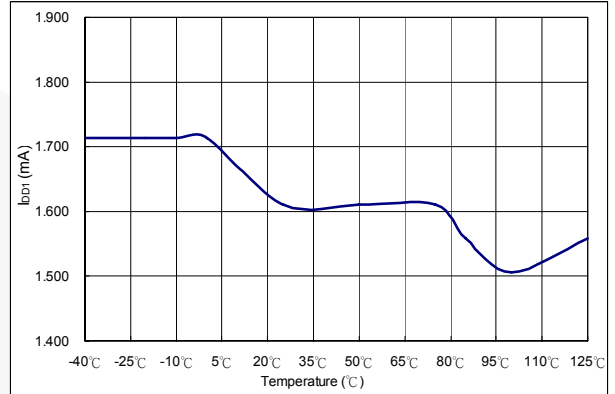


Figure 7. I<sub>D1</sub> vs. T<sub>A</sub>

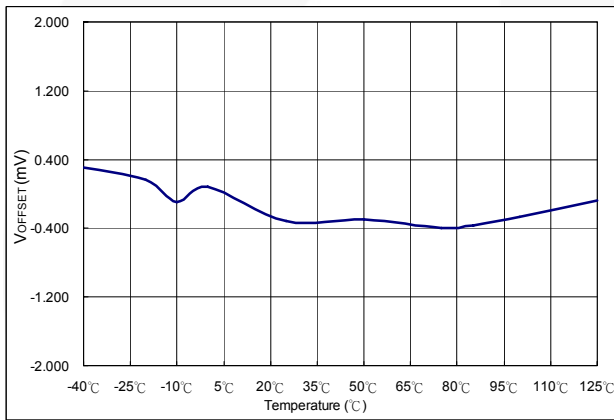


Figure 8. V<sub>OFFSET</sub> vs. T<sub>A</sub>

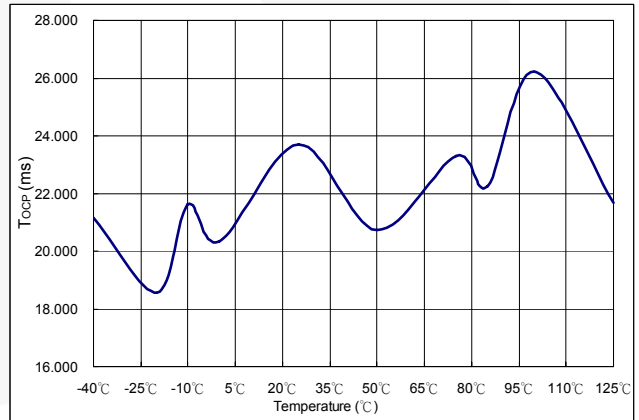


Figure 9. t<sub>OCP</sub> vs. T<sub>A</sub>

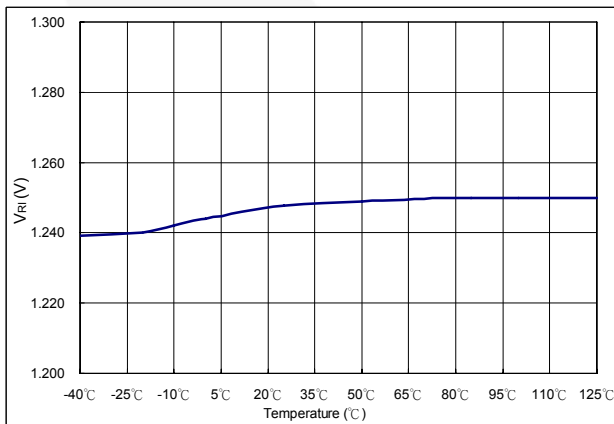


Figure 10. V<sub>RI</sub> vs. T<sub>A</sub>

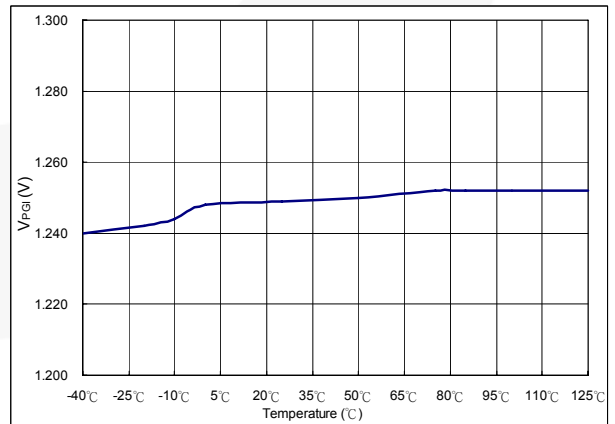


Figure 11. V<sub>PGI</sub> vs. T<sub>A</sub>

## Physical Dimensions

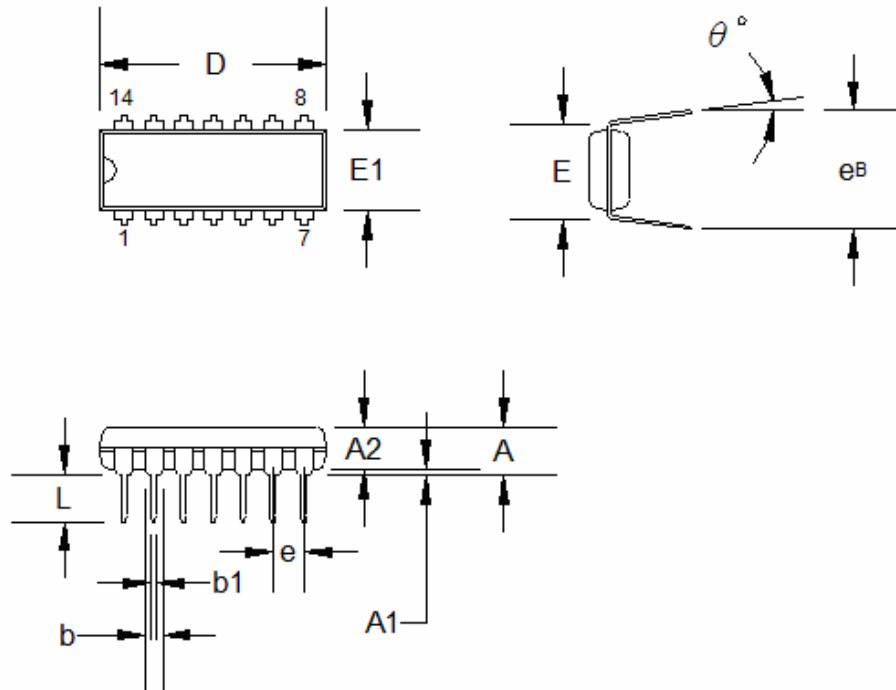


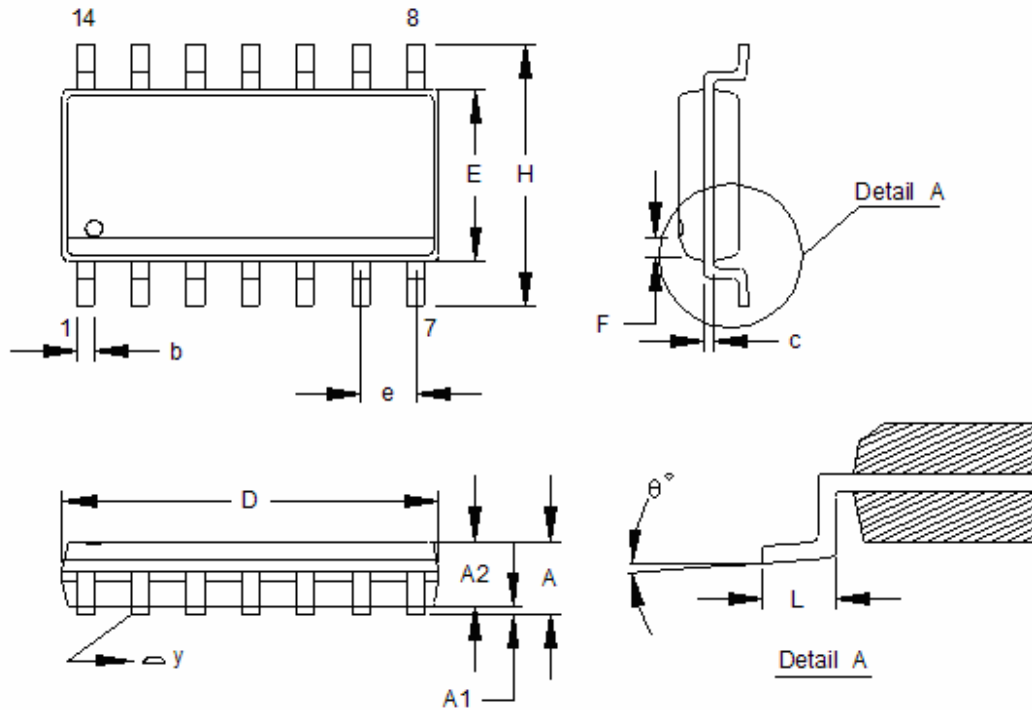
Figure 12. 14-PDIP

Symbol	Millimeter			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.334			0.210
A1	0.381			0.015		
A2	3.175	3.302	3.429	0.125	0.130	0.135
b		1.524			0.060	
b1		0.457			0.018	
D	18.669	19.177	19.685	0.735	0.755	0.775
E		7.620			0.300	
E1	6.121	6.299	6.477	0.241	0.248	0.255
e		2.540			0.100	
L	2.921	3.302	3.810	0.115	0.130	0.150
e <sub>B</sub>	8.509	9.017	9.525	0.335	0.355	0.375
θ°	0°	7°	15°	0°	7°	15°

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:  
<http://www.fairchildsemi.com/packaging/>

**Physical Dimensions** (Continued)



**Figure 13. 14-SOIC**

Symbol	Millimeter			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.346		1.753	0.053		0.069
A1	0.101		0.254	0.004		0.010
A2	1.244		1.499	0.049		0.059
b		0.406			0.016	
c		0.203			0.008	
D	9.804		10.008	0.386		0.394
E	3.810		3.988	0.150		0.157
e		1.270			0.050	
H	5.791		6.198	0.228		0.244
L	0.406		1.270	0.016		0.050
F		0.381X45°			0.015X45°	
y			0.101			0.004
θ°	0°		8°	0°		8°

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:  
<http://www.fairchildsemi.com/packaging/>



**TRADEMARKS**

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

- |   |   |   |   |
|---|---|---|---|
| ACEx <sup>®</sup>   | FPST <sup>™</sup>   | PDP SPM <sup>™</sup>  | The Power Franchise <sup>®</sup>  |
| Build it Now <sup>™</sup>   | F-PFS <sup>™</sup>  | Power-SPM <sup>™</sup>  |  |
| CorePLUS <sup>™</sup>   | FRFET <sup>®</sup>  | PowerTrench <sup>®</sup>  | TinyBoost <sup>™</sup>  |
| CorePOWER <sup>™</sup>  | Global Power Resource <sup>SM</sup>   | Programmable Active Droop <sup>™</sup>  | TinyBuck <sup>™</sup>   |
| CROSSVOLT <sup>™</sup>  | Green FPST <sup>™</sup>   | QFET <sup>®</sup>   | TinyLogic <sup>®</sup>  |
| CTL <sup>™</sup>  | Green FPST <sup>™</sup> e-Series <sup>™</sup>                                     | QS <sup>™</sup>   | TINYOPTO <sup>™</sup>   |
| Current Transfer Logic <sup>™</sup>   | GTQ <sup>™</sup>  | Quiet Series <sup>™</sup>   | TinyPower <sup>™</sup>  |
| EcoSPARK <sup>®</sup>   | IntelliMAX <sup>™</sup>   | RapidConfigure <sup>™</sup>   | TinyPWM <sup>™</sup>  |
| EfficientMax <sup>™</sup>   | ISOPLANAR <sup>™</sup>  | Saving our world, 1mW at a time <sup>™</sup>                                      | TinyWire <sup>™</sup>   |
| EZSWITCH <sup>™</sup> *   | MegaBuck <sup>™</sup>   | SmartMax <sup>™</sup>   | μSerDes <sup>™</sup>  |
|  | MICROCOUPLER <sup>™</sup>   | SMART START <sup>™</sup>  |  |
|  | MicroFET <sup>™</sup>   | SPM <sup>®</sup>  | UHC <sup>®</sup>  |
| Fairchild <sup>®</sup>  | MicroPak <sup>™</sup>   | STEALTH <sup>™</sup>  | Ultra FRFET <sup>™</sup>  |
| Fairchild Semiconductor <sup>®</sup>  | MillerDrive <sup>™</sup>  | SuperFET <sup>™</sup>   | UniFET <sup>™</sup>   |
| FACT Quiet Series <sup>™</sup>  | MotionMax <sup>™</sup>  | SuperSOT <sup>™</sup> -3  | VCX <sup>™</sup>  |
| FACT <sup>®</sup>   | Motion-SPM <sup>™</sup>   | SuperSOT <sup>™</sup> -6  | VisualMax <sup>™</sup>  |
| FAST <sup>®</sup>   | OPTOLOGIC <sup>®</sup>  | SuperSOT <sup>™</sup> -8  |   |
| FastvCore <sup>™</sup>  | OPTOPLANAR <sup>®</sup>   | SupreMOS <sup>™</sup>   |   |
| FlashWriter <sup>®</sup> *  |  | SyncFET <sup>™</sup>  |   |
|   |   |  |   |

\* EZSWITCH<sup>™</sup> and FlashWriter<sup>®</sup> are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

**DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. 134