Precision Adjustable Current-Limited, Power-Distribution Switches

Check for Samples: TPS2554, TPS2555

FEATURES

- **Meets USB Current-Limiting Requirements**
- **Adjustable Current Limit, 500 mA to 2.5 A (typ)**
- **Two Independently-Settable, Current-Limit Thresholds**
- **Fast Overcurrent Response - 1.5 µs (typ)**
- **73-mΩ High-Side MOSFET**
- **3.8-µA Maximum Standby Supply Current**
- **PowerPAD™ Thermal Management**
- **Automatic Output Discharge when Disabled**
- **Both High-Enable (TPS2554) and Low-Enable (TPS2555) Versions Available**

APPLICATIONS

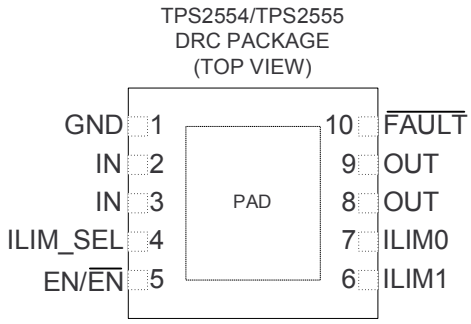
- **USB Ports/Hubs**
- **Digital TV**
- **Set-Top Boxes**
- **VOIP Phones**

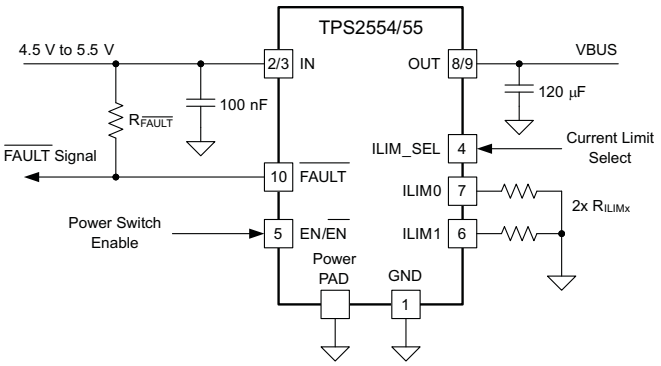
DESCRIPTION

The TPS2554/55 power-distribution switches are intended for applications where precision current limiting is required or heavy capacitive loads and short circuits are encountered. These devices offer a programmable current-limit threshold between 500 mA and 2.5 A (typ) via an external resistor.

TPS2554/55 devices limit the output current to a safe level by switching into a constant-current mode when the output load exceeds the current-limit threshold. The $\overline{\text{FAULT}}$ logic output asserts low during overcurrent and over-temperature conditions.

TPS2554/55 DRC Package and Typical Application Diagram





This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1) (2)

			VALUE	UNIT
	Voltage range on IN, OUT, EN or $\overline{EN}$, ILIM0, ILIM1, ILIM_SEL, $\overline{FAULT}$		–0.3 to 7	V
	Voltage range from IN to OUT		–7 to 7	
I_{OUT}	Continuous output current		Internally limited	
	Continuous total power dissipation		Internally limited	
	Continuous $\overline{FAULT}$ sink current		25	mA
	ILIM source current		Internally limited	
	ESD	HBM	2	kV
		CDM	500	V
T_J	Maximum junction temperature		–40 to OTSD2(3)	°C
T_{stg}	Storage temperature range		-65 to 150	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltages are referenced to GND unless otherwise noted.
(3) Ambient over-temperature shutdown threshold.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{IN}	Input voltage, IN	4.5	5.5	V
V_{EN} , $V_{\overline{EN}}$, ILIM_SEL	Logic-level inputs	0	5.5	
I_{OUT}	Continuous output current, OUT	0	2.5	A
T_J	Operating virtual junction temperature	–40	125	°C
R_{ILIM}	Recommended resistor limit range	16.9	750	kΩ

THERMAL INFORMATION

THERMAL METRIC(1)		TPS2554/TPS2555 DRC 14 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	45.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	53.4	
θ_{JB}	Junction-to-board thermal resistance(4)	21.4	
ψ_{JT}	Junction-to-top characterization parameter(5)	1.0	
ψ_{JB}	Junction-to-board characterization parameter(6)	21.6	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	5.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

Conditions are -40°C ≤ T_J ≤ 125°C unless otherwise noted V_{EN} (if TPS2554) = V_{IN} = 5 V, $V_{\overline{EN}}$ (if TPS2555) = 0 V, $R_{\overline{FAULT}}$ = 10 kΩ, R_{ILIM0} = 210 kΩ, R_{ILIM1} = 20 kΩ, ILIM_SEL = 0 V unless otherwise noted. Positive currents are into pins. Typical values are at 25 °C. All voltages are with respect to GND unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Power Switch							
$R_{DS(on)}$	Static drain-source on-state resistance	I_{OUT} = 2 A, V_{ILIM_SEL} = Logic HI			73	120	mΩ
		I_{OUT} = 100 mA, V_{ILIM_SEL} = Logic LO			73	120	
		-40 °C ≤ T_A = T_J ≤ 85 °C, I_{OUT} = 2 A, V_{ILIM_SEL} = Logic HI			73	105	
		T_A = T_J = 25 °C, I_{OUT} = 2 A, V_{ILIM_SEL} = Logic HI			73	84	
t_r	Rise time, output	C_L = 1 µF, R_L = 100 Ω			1	1.5	ms
t_f	Fall time, output	C_L = 1 µF, R_L = 100 Ω		0.2		0.5	
R_{DIS}	OUT discharge resistance			400	500	630	Ω
I_{REV}	Reverse leakage current	V_{OUT} = 5.5 V, V_{IN} = V_{EN} = 0 V or V_{OUT} = $V_{\overline{EN}}$ = 5.5 V, V_{IN} = 0 V, T_J = 25 °C			0	1	µA
Enable Input EN (TPS2554), $\overline{\text{Enable}}$ Input $\overline{\text{EN}}$ (TPS2555)							
V_{EN}, $V_{\overline{EN}}$	EN, $\overline{EN}$ pin threshold, falling			0.9	1.1	1.65	V
V_{EN_HYS}	EN, $\overline{EN}$ Hysteresis				200		mV
I_{EN}, $I_{\overline{EN}}$	Input current	V_{EN}, $V_{\overline{EN}}$ = 0 V or 5.5 V		-0.5		0.5	µA
t_{ON}	Turn-on time	C_L = 1 µF, R_L = 100 Ω			3.4	5	ms
t_{OFF}	Turn-off time	C_L = 1 µF, R_L = 100 Ω			1.7	3	
Current Limit							
V_{ILIM_SEL}	ILIM_SEL threshold, falling			0.9	1.1	1.65	V
V_{ILIM_HYS}	I_{LIM_SEL} Hysteresis				200		mV
	ILIM_SEL input current	V_{ILIM_SEL} = 0 V or 5.5 V		-0.5		0.5	µA
I_{SHORT}	Maximum DC output current from IN to OUT	V_{ILIM_SEL} = Logic LO	R_{ILIM0} = 210 kΩ	185	230	265	mA
			R_{ILIM0} = 100 kΩ	420	480	530	
		V_{ILIM_SEL} = Logic HI	R_{ILIM1} = 20 kΩ	2150	2430	2650	
			R_{ILIM1} = 16.9 kΩ	2550	2840	3100	
t_{IOS}	Response time to short circuit	V_{IN} = 5.0 V			1.5		µs
Supply Current							
I_{CCL}	Supply current, switch disabled	V_{EN} = 0 V, $V_{\overline{EN}}$ = V_{IN}; OUT grounded; -40 °C ≤ T_J ≤ 85 °C			0.1	3.8	µA
I_{CCH}	Supply current, operating	V_{EN} = 0 V, $V_{\overline{EN}}$ = V_{IN}			90	115	
			V_{ILIM_SEL} = Logic HI		110	135	
Undervoltage Lockout							
V_{UVLO}	Low-level input voltage, IN	V_{IN} rising		3.9	4.1	4.3	V
	Hysteresis, IN				100		mV
$\overline{\text{FAULT}}$							
	Output low voltage, $\overline{FAULT}$	$I_{\overline{FAULT}}$ = 1 mA				100	mV
	Off-state leakage	$V_{\overline{FAULT}}$ = 5.5 V				1	µA
	$\overline{FAULT}$ deglitch	$\overline{FAULT}$ assertion or negation due to overcurrent condition		5	8.5	12	ms
Thermal Shutdown							
	Thermal shutdown threshold			155			°C
	Thermal shutdown threshold in current-limit			135			
	Hysteresis				10		

Parameter Measurement Information

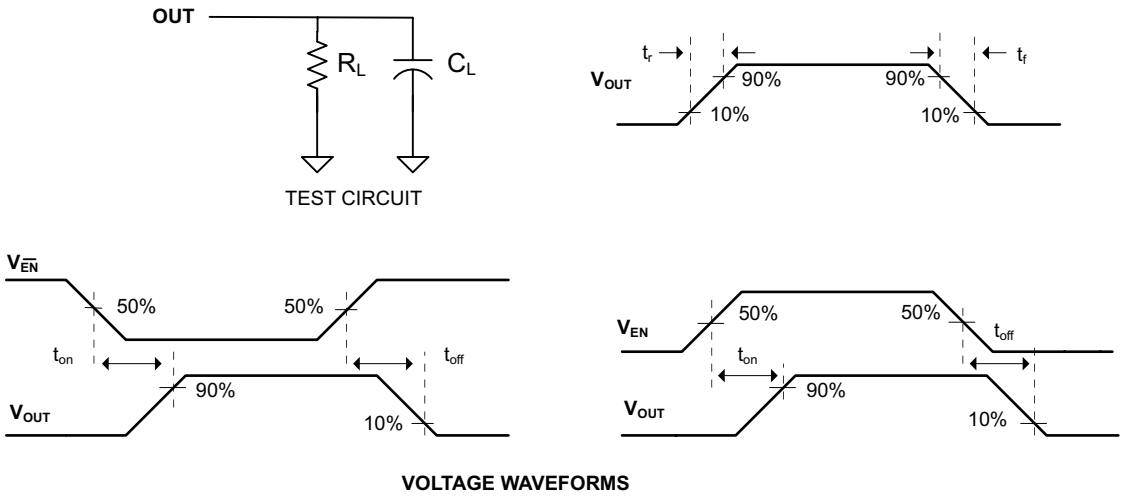


Figure 1. Test Circuit and Voltage Waveforms

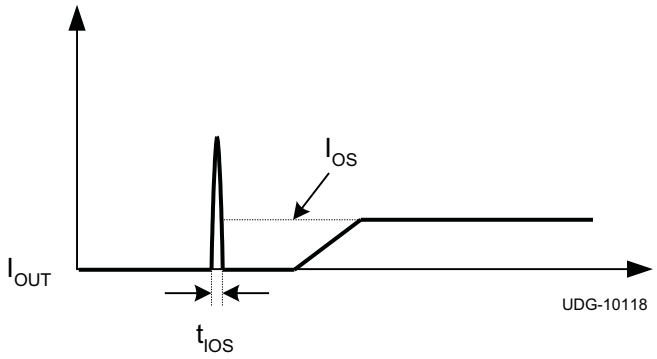


Figure 2. Response Time to Short-Circuit Waveform

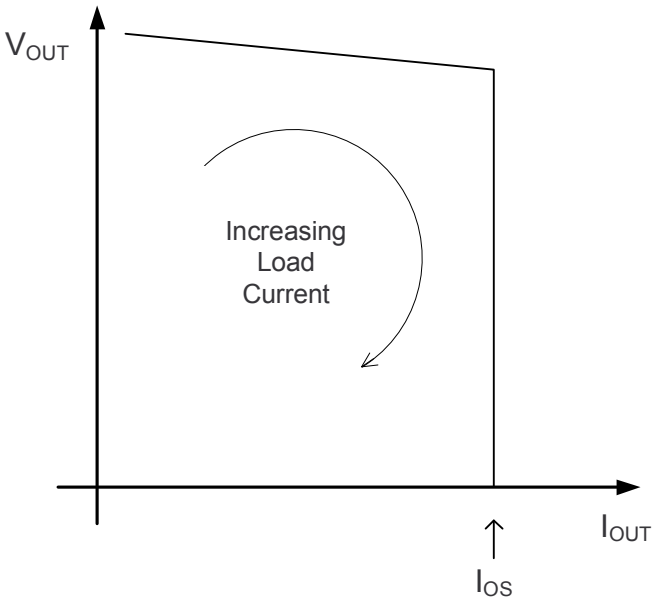


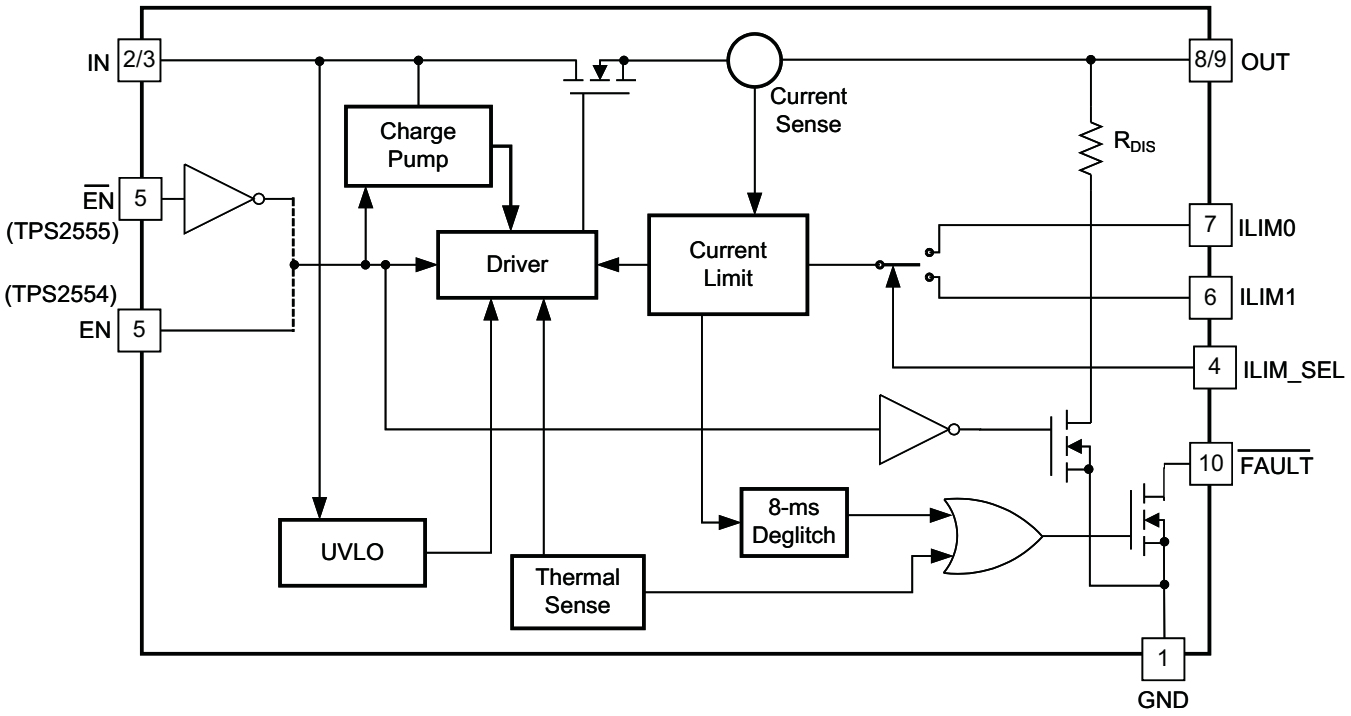
Figure 3. Output Voltage vs Output Current Behavior

DEVICE INFORMATION

Pin Functions

PIN			I/O	DESCRIPTION
NAME	TPS2554	TPS2555		
EN	5	-	I	Enable input, logic high turns on power switch (TPS2554).
$\overline{EN}$	-	5	I	Enable input, logic low turns on power switch (TPS2555).
GND	1	1		Ground connection; connect externally to PowerPAD™.
IN	2, 3	2, 3	I	Input voltage; connect a 100-nF, or greater, ceramic capacitor from IN to GND as close to the device as possible.
$\overline{FAULT}$	10	19	O	Active-low, open-drain output, asserted during overcurrent or over-temperature conditions.
OUT	8, 9	8, 9	O	Power-switch output
ILIM0	7	7	I	External resistor used to set current-limit threshold when ILIM_SEL = LO
ILIM1	6	6	I	External resistor used to set current-limit threshold when ILIM_SEL = HI
ILIM_SEL	4	4	I	Logic-level input that selects between ILIM0 and ILIM1 current-limit threshold setting
PowerPAD™	–	–		Internally connected to GND; used to heat-sink the device to the circuit board traces. Connect PowerPAD™ to GND pin externally.

TPS2554/TPS2555 Functional Block Diagram



TYPICAL CHARACTERISTICS

In UVLO Rising vs Temperature

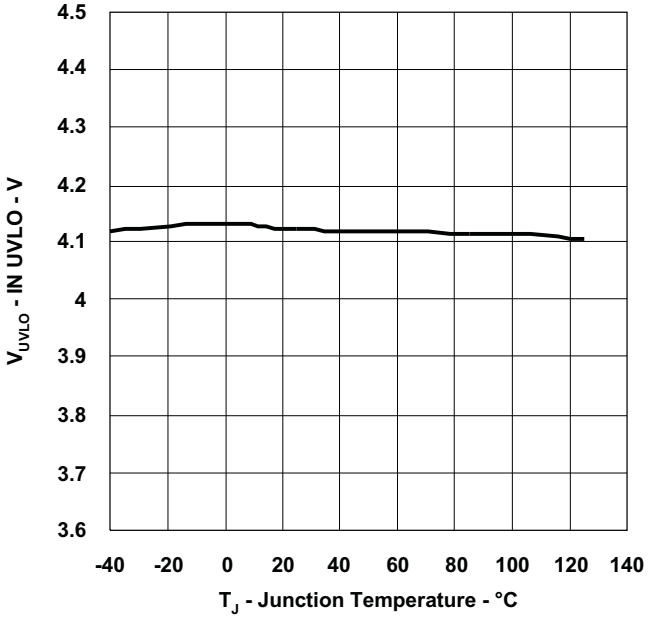


Figure 4.

Supply Current - Disabled vs Temperature

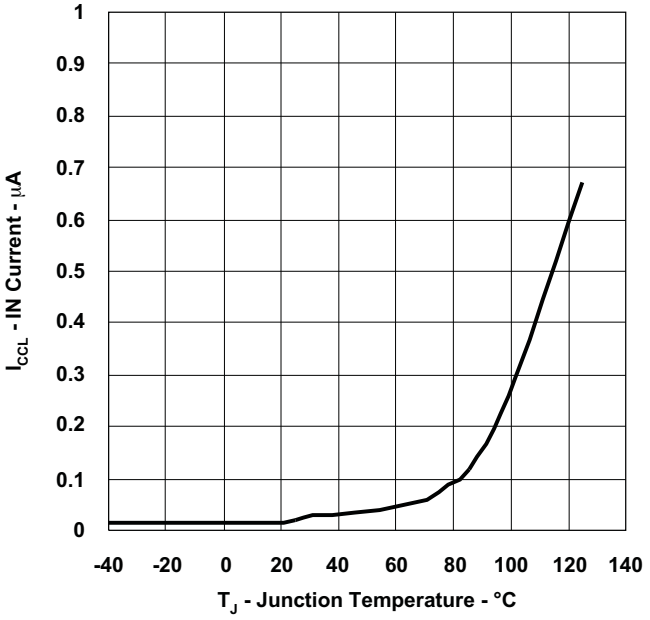


Figure 5.

Supply Current vs Temperature

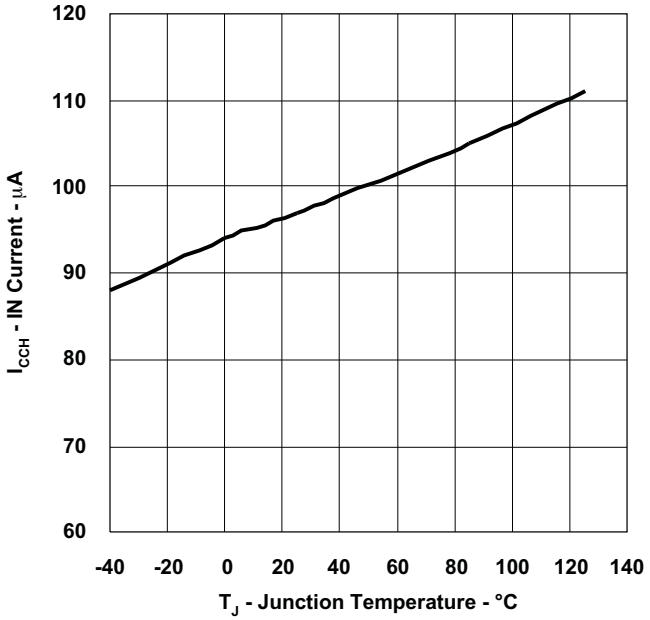


Figure 6.

Current Limit vs Current Limit Resistance

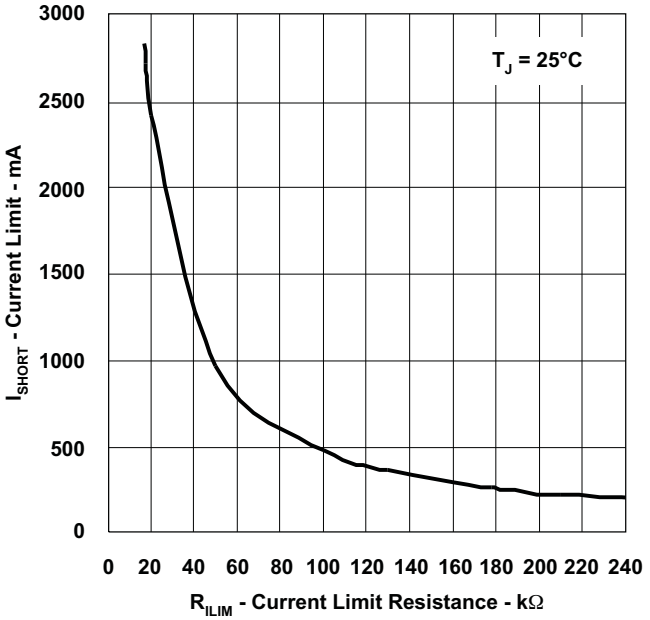


Figure 7.

TYPICAL CHARACTERISTICS (continued)

Current Limit vs Temperature

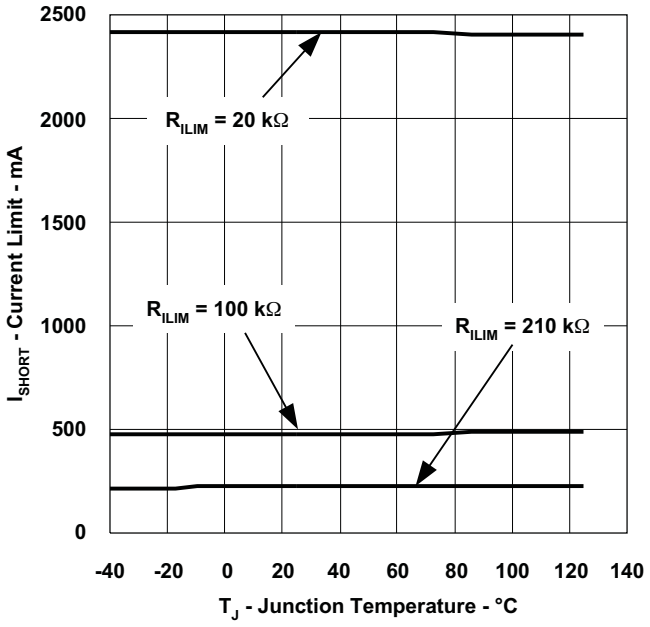


Figure 8.

Power Switch On-Resistance vs Temperature

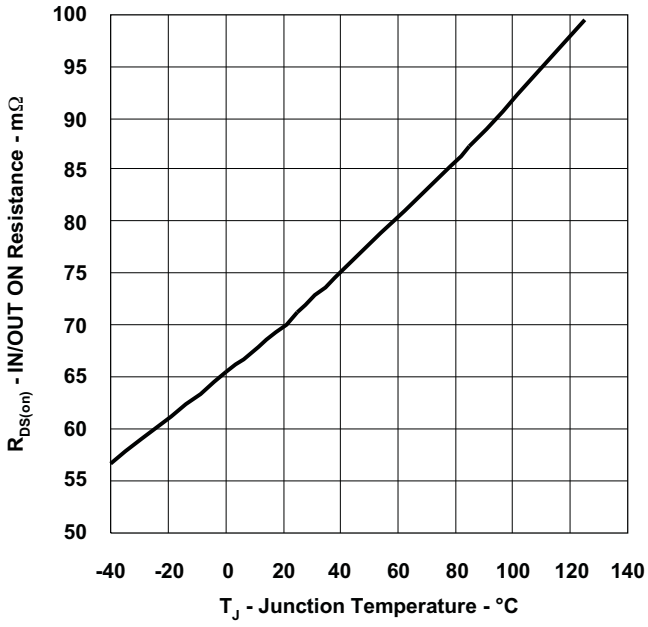


Figure 9.

Turn-On Time, Turn-Off Time vs Temperature

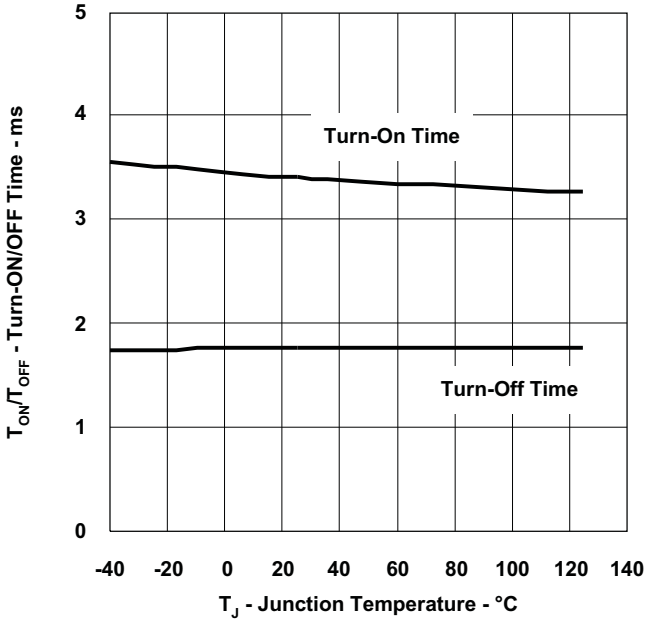


Figure 10.

Fault Output Voltage vs Sink Current

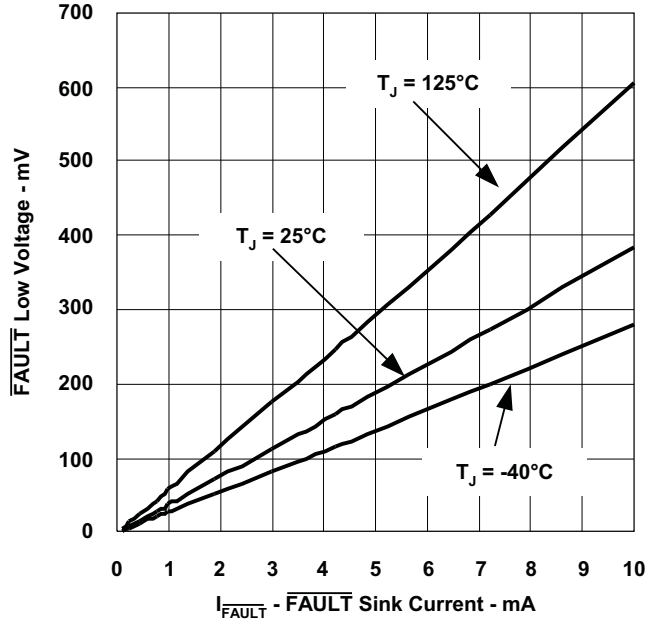


Figure 11.

TYPICAL CHARACTERISTICS (continued)

EN Threshold Falling vs Temperature

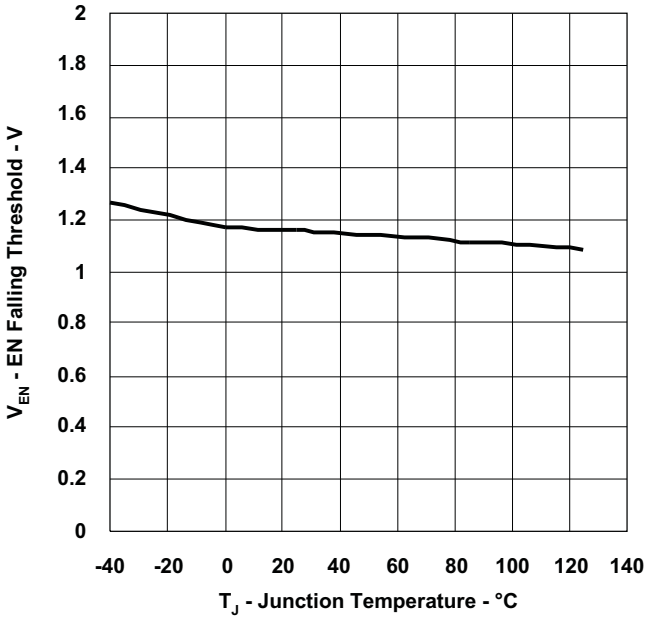


Figure 12.

Response to a Short Circuit (following assertion of enable)

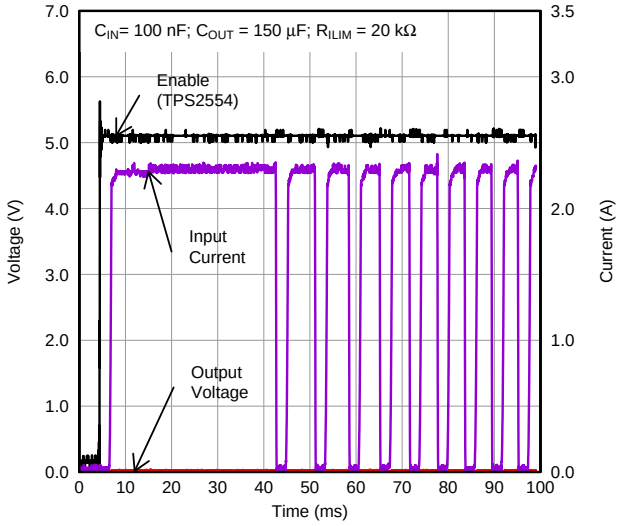


Figure 13.

Response to a Short Circuit (apply input voltage with output shorted)

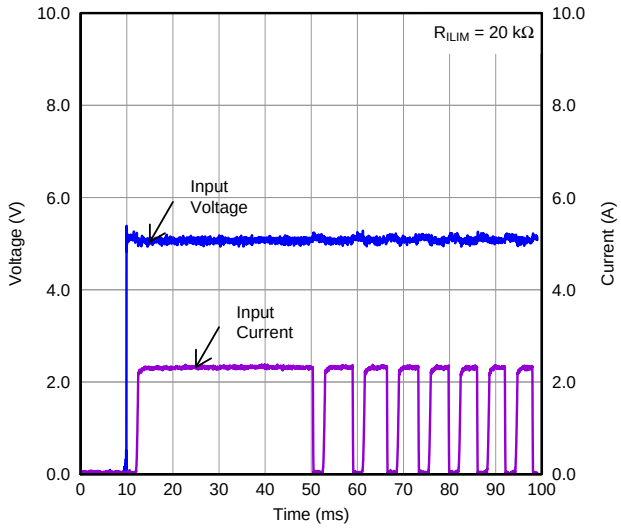


Figure 14.

Response to a Short Circuit (apply input voltage with output shorted)

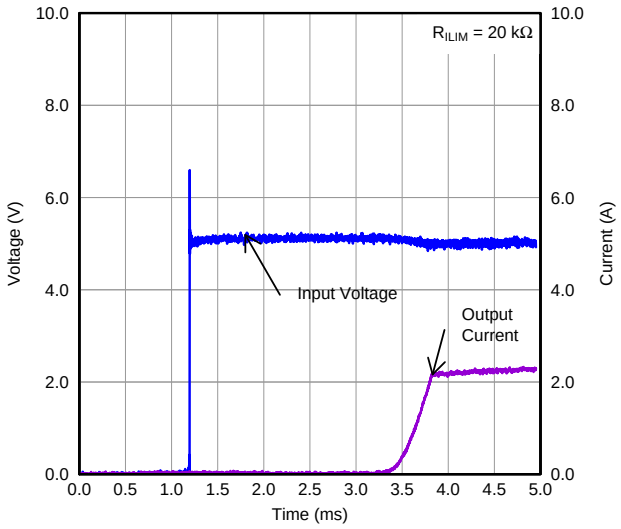


Figure 15.

TYPICAL CHARACTERISTICS (continued)

Response to a Short Circuit (from a no-load condition)

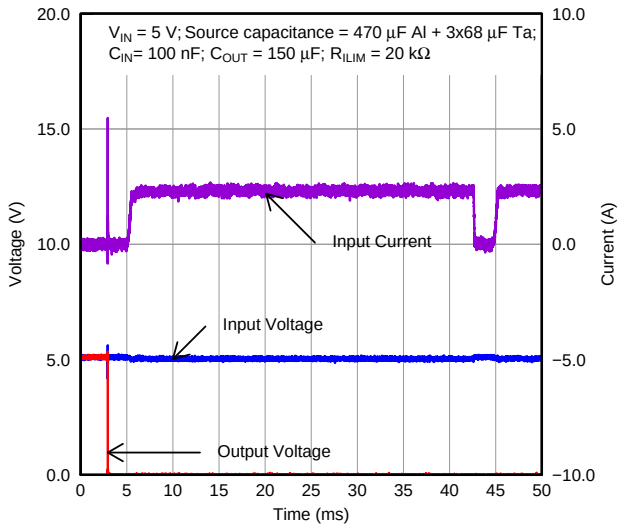


Figure 16.

Response to a Short Circuit (from a no-load condition)

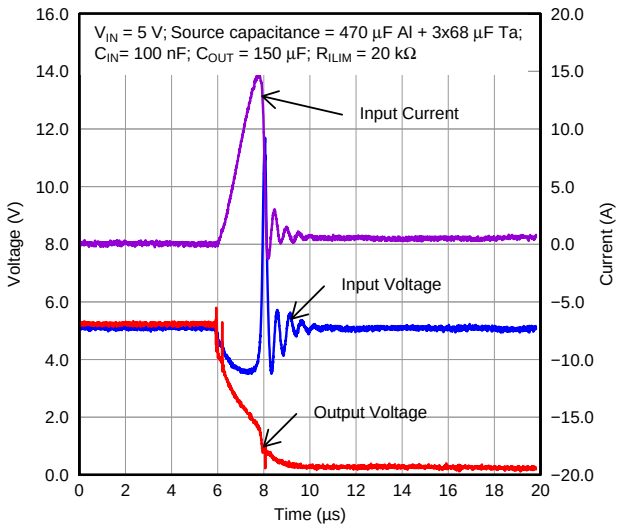


Figure 17.

DETAILED DESCRIPTION

Overview

The TPS2554/55 is a current-limited, power-distribution switch using an internal N-channel MOSFET as a switch for applications where short circuits or heavy-capacitive loads will be encountered. This device allows the user to program two independent current-limit thresholds between 500 mA and 2.5 A (typ) via two external resistors. The ILIM_SEL pin allows the user to select one current limit or the other. This device incorporates an internal charge pump and the gate-drive circuitry necessary to drive the N-channel MOSFET. The charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The driver controls the gate voltage of the power switch. The TPS2554/55 family limits the output current to the programmed current-limit threshold I_{LIM0} or I_{LIM1} during an overcurrent or short-circuit event by reducing the charge-pump voltage driving the N-channel MOSFET and operating it in the linear range of operation. This necessarily results in a reduction in the output voltage at OUT. Exposure to an overload condition leads directly to heat dissipation in the internal MOSFET. The MOSFET is protected thermally such that it will shut off when it gets too hot. The TPS2554/55 will automatically restart following cooling of the device.

Overcurrent Conditions

The TPS2554/55 responds to overcurrent conditions by limiting the output current to the short-circuit current set by R_{ILIM0} or R_{ILIM1}, whichever is selected at the ILIM_SEL pin. When an overcurrent condition is detected the device maintains a constant output current, and the output voltage reduces accordingly. Two possible overload conditions can occur.

The first condition is when a short circuit or partial short circuit is present when the device is powered-up or enabled. The output voltage is held near zero potential with respect to ground and the TPS2554/55 ramps the output current to the selected output current, I_{LIM0} or I_{LIM1}. The TPS2554/55 will limit the current to the selected limit until the overload condition is removed or heating of the internal MOSFET forces a shutdown. (Following thermal shutdown the TPS2554/55 cools and another start-up attempt occurs automatically.)

The second condition is when a short circuit, partial short circuit, or transient overload occurs while the device is enabled and powered on. In response to the load transient the output current will typically overshoot the selected current limit during t_{IOS} as the TPS2554/55 turns off the pass device. Then, the current-sense amplifier will recover and the output current will be maintained at the selected current limit. As in the previous case, the TPS2554/55 will maintain the current limit until the overload condition is removed or the device begins to thermal cycle.

The TPS2554/55 thermal cycles if an overload condition is present long enough to activate thermal limiting in any of the above cases. The device turns off when the junction temperature exceeds 135°C (min) while in current limit. The device remains off until the junction temperature cools 20°C (typ) and then restarts. The TPS2554/55 cycles on/off until the overload is removed.

Current-Limit Thresholds

The TPS2554/5 has two independent current-limit thresholds that are each programmed externally with a resistor. The following equation programs the typical current-limit threshold:

$$I_{SHORT} = \frac{48000}{R_{ILIMx}} \quad (1)$$

where

- I_{SHORT} = Current-limit threshold, mA
- R_{ILIM} = Resistance at ILIMx pin, kΩ

R_{ILIMx} corresponds to R_{ILIM0} when ILIM_SEL is logic LO and to R_{ILIM1} when ILIM_SEL is logic HI. The ILIM_SEL pin allows the system to digitally select between two current-limit thresholds, which is useful, for example, in end equipment that may require a lower setting when powered from batteries versus wall adapters.

$\overline{\text{FAULT}}$ Response

The $\overline{\text{FAULT}}$ open-drain output is asserted low during an overcurrent or over-temperature condition. The TPS2554/55 asserts the $\overline{\text{FAULT}}$ signal until the fault condition is removed and the device resumes normal operation. The TPS2554/55 is designed to eliminate false $\overline{\text{FAULT}}$ reporting by using an internal delay "deglitch" circuit for overcurrent conditions (9 ms typical) without the need for external circuitry. This ensures that $\overline{\text{FAULT}}$ is not accidentally asserted due to normal operation such as starting into a heavy capacitive load. The deglitch circuitry delays entering and leaving current-limit-induced fault conditions. The $\overline{\text{FAULT}}$ signal is not deglitched when the MOSFET is disabled due to an over-temperature condition, but it is deglitched after the device has cooled and begins to turn on. This unidirectional deglitch feature prevents FAULT oscillation during an over-temperature event.

Undervoltage Lockout (UVLO)

The Undervoltage Lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold (4.1 V, nominal). Built-in hysteresis prevents unwanted on/off cycling due to input-voltage droop during turn on.

Enable (EN OR $\overline{\text{EN}}$)

The logic enable controls the power switch and device supply current. The supply current is reduced to less than 3.8 µA when a logic low is present on EN (TPS2554) or when a logic high is present on $\overline{\text{EN}}$ (TPS2555). A logic high input on EN or a logic low input on $\overline{\text{EN}}$ enables the driver, control circuits, and power switch. The enable input is compatible with both TTL and CMOS logic levels.

Output Discharge

When the output is disabled through either the EN (TPS2554) or $\overline{\text{EN}}$ (TPS2555) pin or by an over-temperature shutdown the OUT pin is discharged internally through a MOSFET. Nominal MOSFET resistance (R_{DIS}) is 500 Ω.

Thermal Sense

The TPS2554/55 self protects by using two independent thermal-sensing circuits that monitor the operating temperature of the power switch and will disable operation if the temperature exceeds recommended operating conditions. The TPS2554/55 device operates in constant-current mode during an overcurrent condition thereby increasing the voltage drop across the MOSFET power switch. The power dissipation in the package increases with the voltage drop across the power switch, thereby causing the junction temperature to rise during an overcurrent condition. The first thermal sensor turns off the power switch when the die temperature exceeds 135°C (min) and the part is in current limit. Hysteresis is built into the thermal sensor, and the switch turns on after the device has cooled approximately 20°C. The TPS2554/55 continues to cycle off and on until the fault is removed.

The TPS2554/55 also has a second ambient thermal sensor. The ambient thermal sensor turns off the power switch when the die temperature exceeds 155°C (min) regardless of whether the power switch is in current limit and will turn on the power switch back on after the device has cooled approximately 20°C. The TPS2554/55 will continue to cycle off and on until the fault is removed.

APPLICATION INFORMATION

Input and Output Capacitance

Capacitance added to the input and output of the TPS2554/55 improves the performance of the device; the actual capacitance should be optimized for the particular application. For all applications, a 100 nF or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise decoupling. This precaution reduces ringing on the input due to power-supply transients. Additional input capacitance may be needed on the input to prevent voltage overshoot from exceeding the absolute-maximum voltage of the device during heavy transient conditions. This is especially important during bench testing when long, inductive cables are used to connect the evaluation board to the bench power supply.

Output capacitance is not required for proper operation of the TPS2554/55, but placing a high-value electrolytic capacitor on the output pin is recommended when large transient currents are expected on the output.

Programming the Current-Limit Threshold

Two overcurrent thresholds are user-programmable via two external resistors. The recommended 1% resistor range for R_{ILIMx} is 16.9 kΩ ≤ R_{ILIM} ≤ 750 kΩ to ensure stability of the internal regulation loop. Best accuracy is obtained with R_{ILIMx} values less than 210 kΩ. Many applications require that the minimum current limit is above a certain current level or that the maximum current limit is below a certain current level, so it is important to consider the tolerance of the overcurrent threshold when selecting a value for R_{ILIMx}. The following equations approximate the resulting overcurrent threshold for a given external resistor value, R_{ILIMx}. Consult the Electrical Characteristics table for specific current-limit settings. Printed-circuit-board traces routing the R_{ILIMx} resistor to the TPS2554/55 should be as short as possible to reduce parasitic effects on the current-limit accuracy.

The equations and the graph below can be used to estimate the minimum and maximum variation of the current-limit threshold for a predefined resistor value. This variation is an approximation only and does not take into account, for example, the resistor tolerance. For examples of more-precise variation of I_{SHORT} refer to the current-limit section of the Electrical Characteristics table.

$$I_{SHORT} = \frac{48000}{R_{ILIMx}} \quad (2)$$

$$I_{SHORT\_min} = \frac{48000}{R_{ILIMx}^{1.037}} \quad (3)$$

$$I_{SHORT\_max} = \frac{48000}{R_{ILIMx}^{0.962}} \quad (4)$$

- I_{SHORT} = Current-limit threshold, mA
- R_{ILIM} = Resistance at ILIMx pin, kΩ

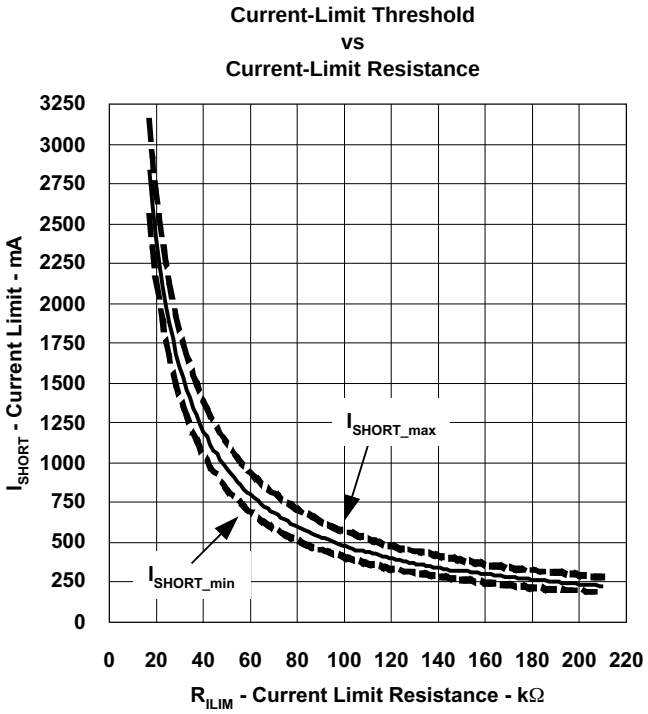


Figure 18.

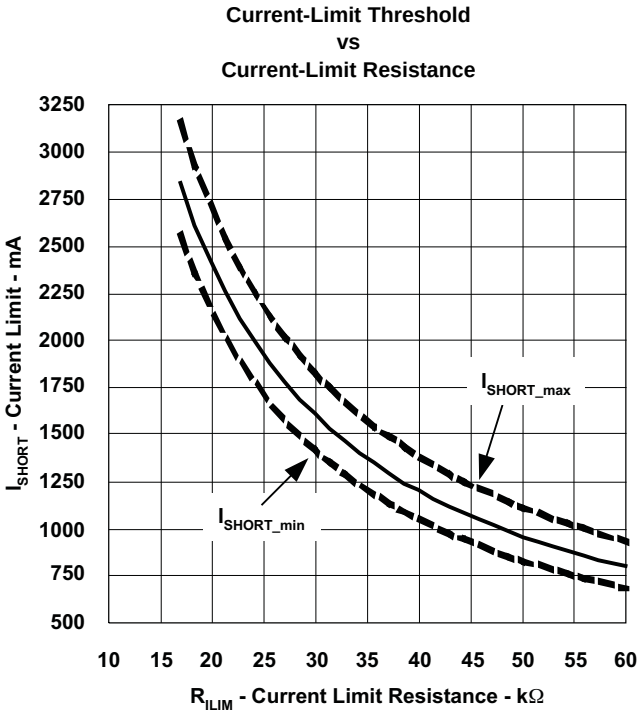


Figure 19.

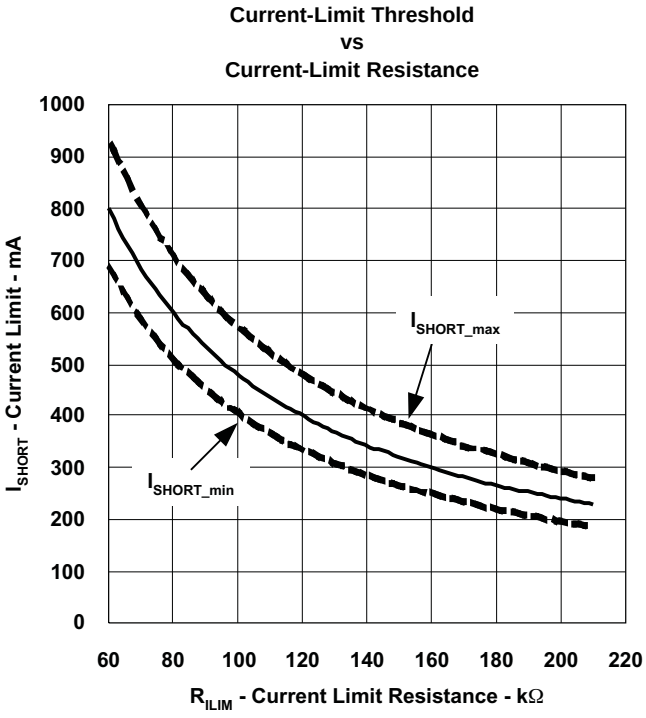


Figure 20.

Current Limit Setpoint Example

In the following example, choose the ILIM resistor to ensure that the TPS2554/55 does not trip off under worst-case conditions of ILIM and resistor tolerance (assume 1% initial-plus-temperature resistor tolerance). For this example IOS_{MIN} = 2500 mA.

$$IOS_{MIN} = \frac{48000}{R_{ILIMx}^{1.037}} = 2500\,mA \tag{5}$$

$$R_{ILIMx} = \left[\frac{48000}{IOS_{MIN}}\right]^{\frac{1}{1.037}} = \left[\frac{48000}{2500\,mA}\right]^{\frac{1}{1.037}} = 17.28\,k\Omega \tag{6}$$

Including resistor tolerance, target maximum:

$$R_{ILIMx} = \frac{17.28k\Omega}{1.01} = 17.11k\Omega \tag{7}$$

Choose:

$$R_{ILIMx} = 16.9k\Omega \tag{8}$$

Layout Guidelines

TPS2554/55 Placement: Place the TPS2554/55 near the USB output connector and 150-µF OUT pin filter capacitor. Connect the exposed PowerPad™ to the GND pin and to the system ground plane using a via array.

IN Pin Bypass Capacitance: Place the 100-nF bypass capacitor near the IN and GND pins, and make the connections using a low-inductance trace.

ILIM0 and ILIM1 Pin Connections: Current-limit, set-point accuracy can be compromised by stray current leakage from a higher voltage source to the ILIM0 or ILIM1 pins. Ensure that there is adequate spacing between IN pin copper/trace and ILIM0 pin trace to prevent contaminant buildup during the PCB assembly process. If a low-current-limit set point is required (R_{ILIMx} > 200 kΩ), use ILIM1 for this case as it is further away from the IN pin.

Power Dissipation and Junction Temperature

The low on resistance of the N-channel MOSFET allows small surface-mount packages to pass large currents. It is good design practice to estimate power dissipation and junction temperature. The below analysis gives an approximation for calculating junction temperature based on the power dissipation in the package. However, it is important to note that thermal analysis is strongly dependent on additional system-level factors. Such factors include air flow, board layout, copper thickness and surface area, and proximity to other devices dissipating power. Good thermal-design practice must include all system-level factors in addition to individual component analysis.

Begin by determining the $R_{DS(on)}$ of the MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $R_{DS(on)}$ from the typical characteristics graph. Using this value, the power dissipation can be calculated by:

- $P_D = R_{DS(on)} \times I_{OUT}^2$

Where:

- P_D = Total power dissipation (W)
- $R_{DS(on)}$ = Power switch on-resistance (Ω)
- I_{OUT} = Maximum current-limit threshold (A)

This step calculates the total power dissipation of the MOSFET.

Finally, calculate the junction temperature:

- $T_J = P_D \times \theta_{JA} + T_A$

Where:

- T_A = Ambient temperature (°C)
- θ_{JA} = Thermal resistance (°C/W)
- P_D = Total power dissipation (W)

Compare the calculated junction temperature with the initial estimate. If they are not within a few degrees, repeat the calculation using a "refined" $R_{DS(on)}$ based on the calculated MOSFET temperature from the previous calculation as the new estimate. Two or three iterations are generally sufficient to achieve the desired result. The final junction temperature is highly dependent on thermal resistance θ_{JA}, and thermal resistance is highly dependent on the individual package and board layout.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2554DRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2554	Samples
TPS2554DRCT	ACTIVE	VSON	DRC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2554	Samples
TPS2555DRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2555	Samples
TPS2555DRCT	ACTIVE	VSON	DRC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2555	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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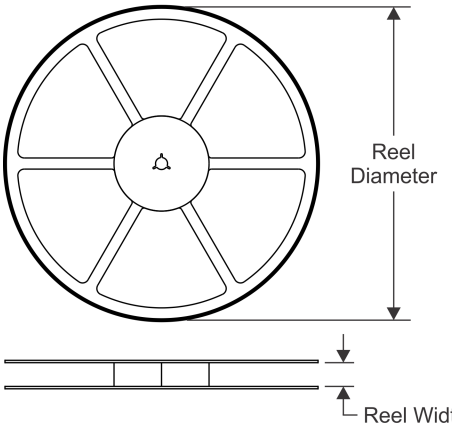
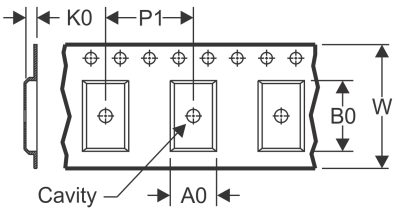
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

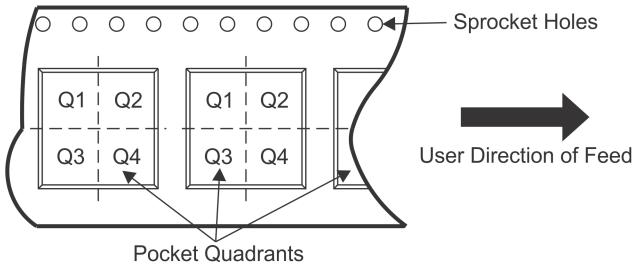


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

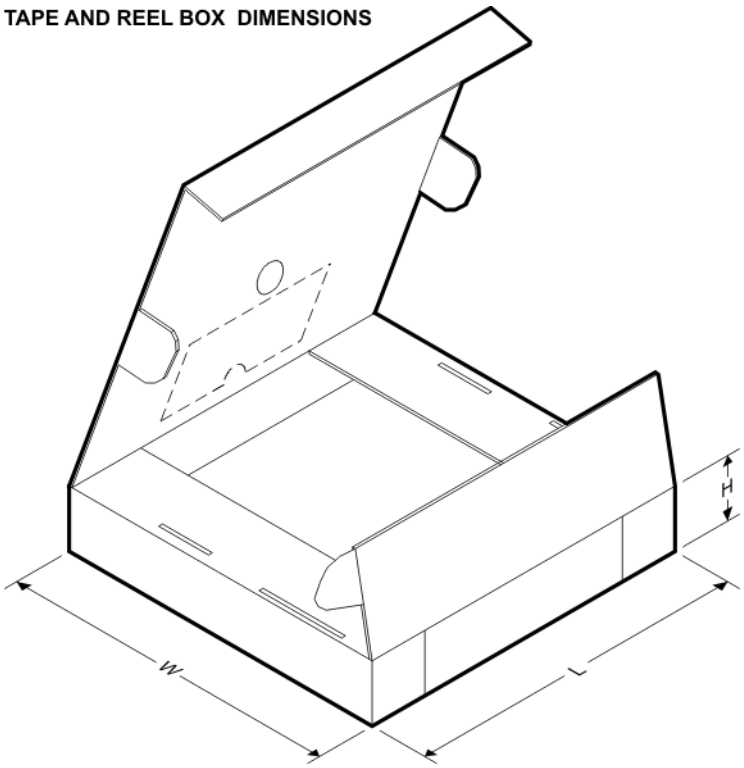
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2554DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2554DRCR	VSON	DRC	10	3000	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2
TPS2554DRCT	VSON	DRC	10	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2
TPS2554DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2555DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2555DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2554DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS2554DRCR	VSON	DRC	10	3000	338.0	355.0	50.0
TPS2554DRCT	VSON	DRC	10	250	338.0	355.0	50.0
TPS2554DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS2555DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS2555DRCT	VSON	DRC	10	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

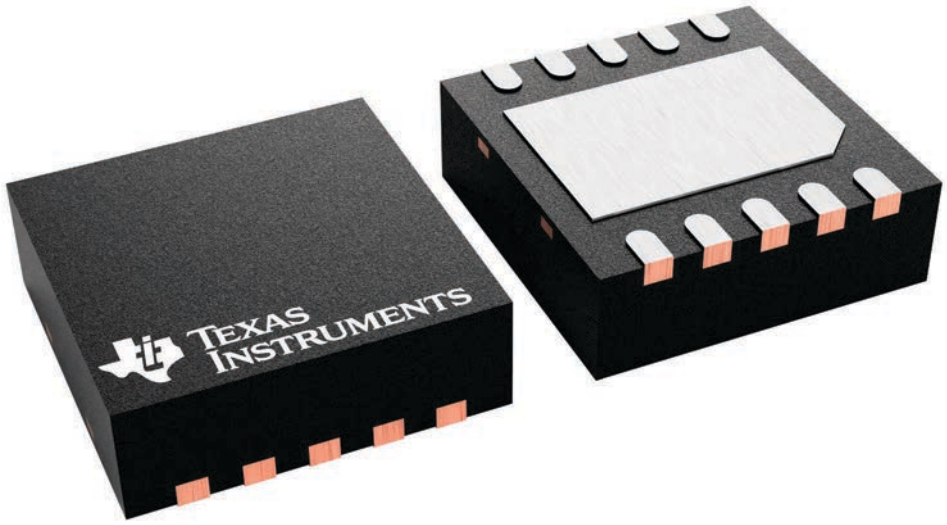
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



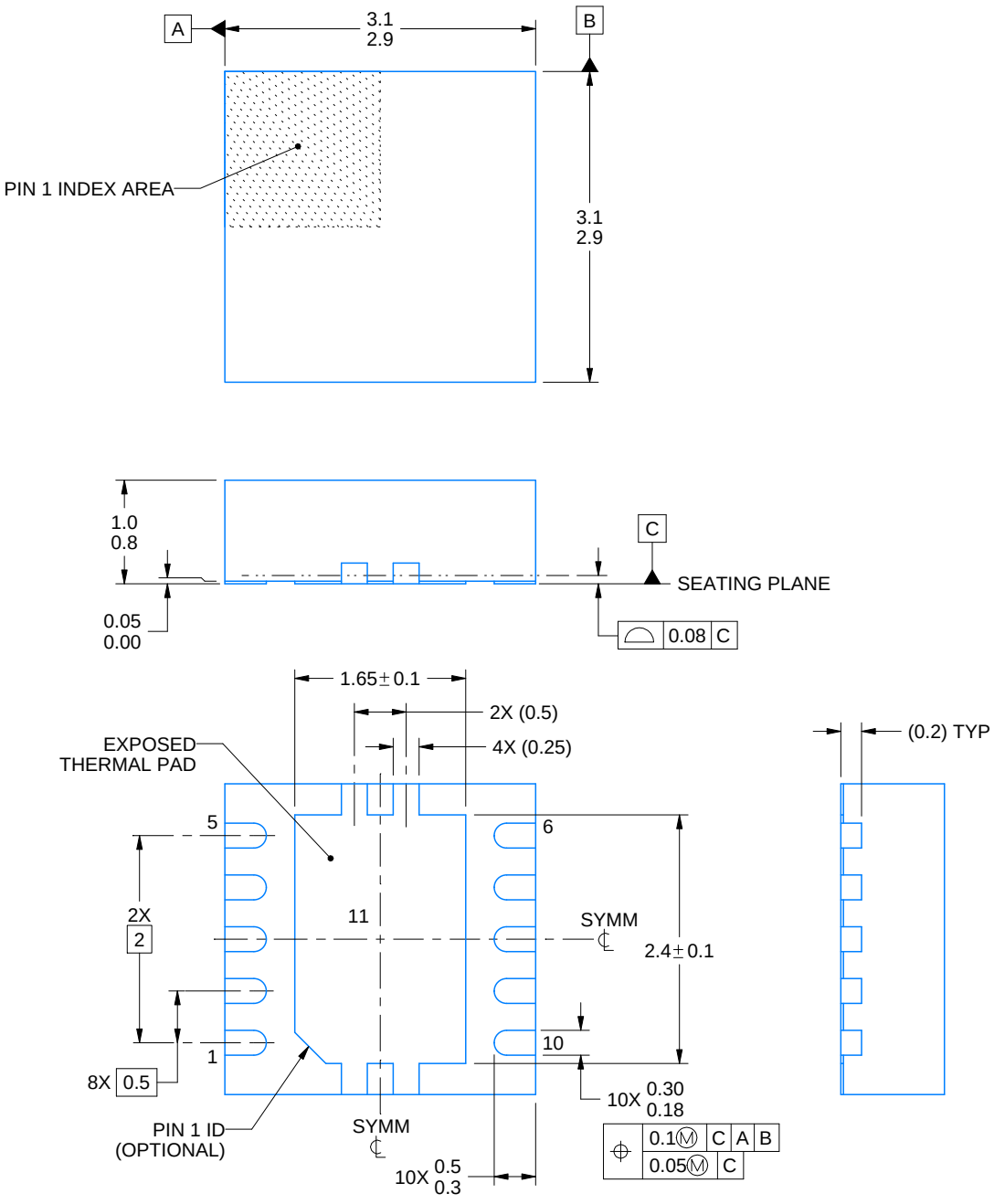
4226193/A

DRC0010J

PACKAGE OUTLINE

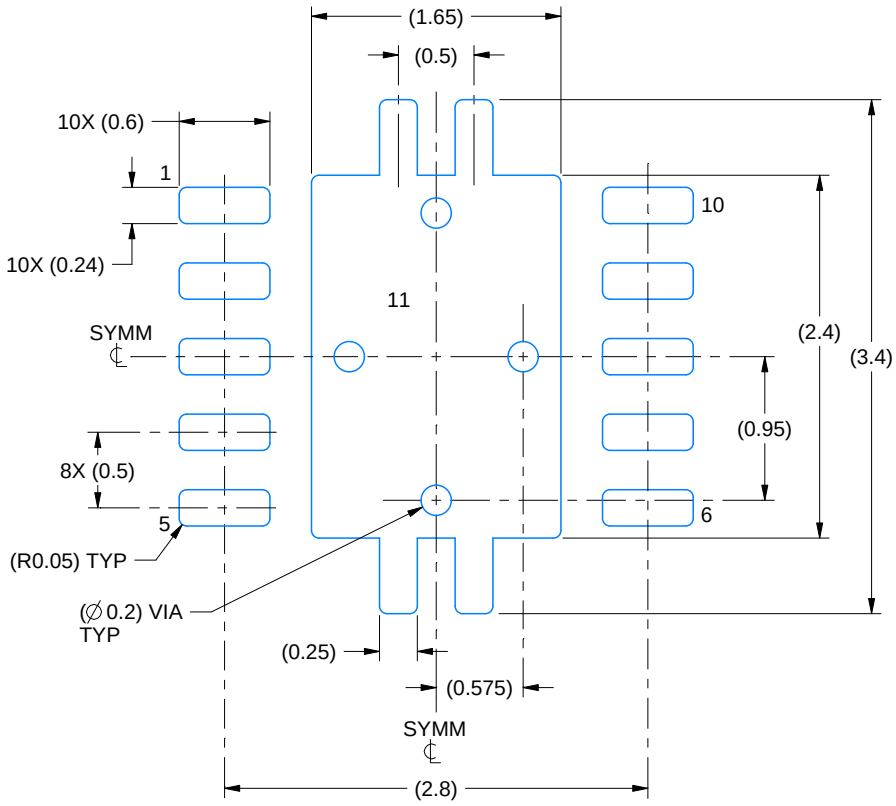
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

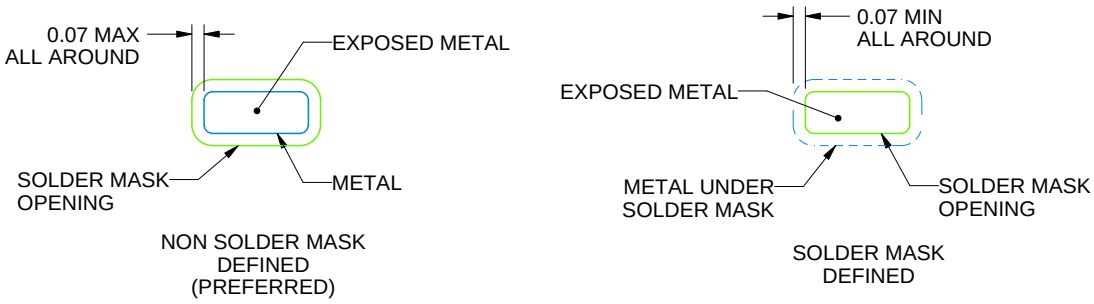


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

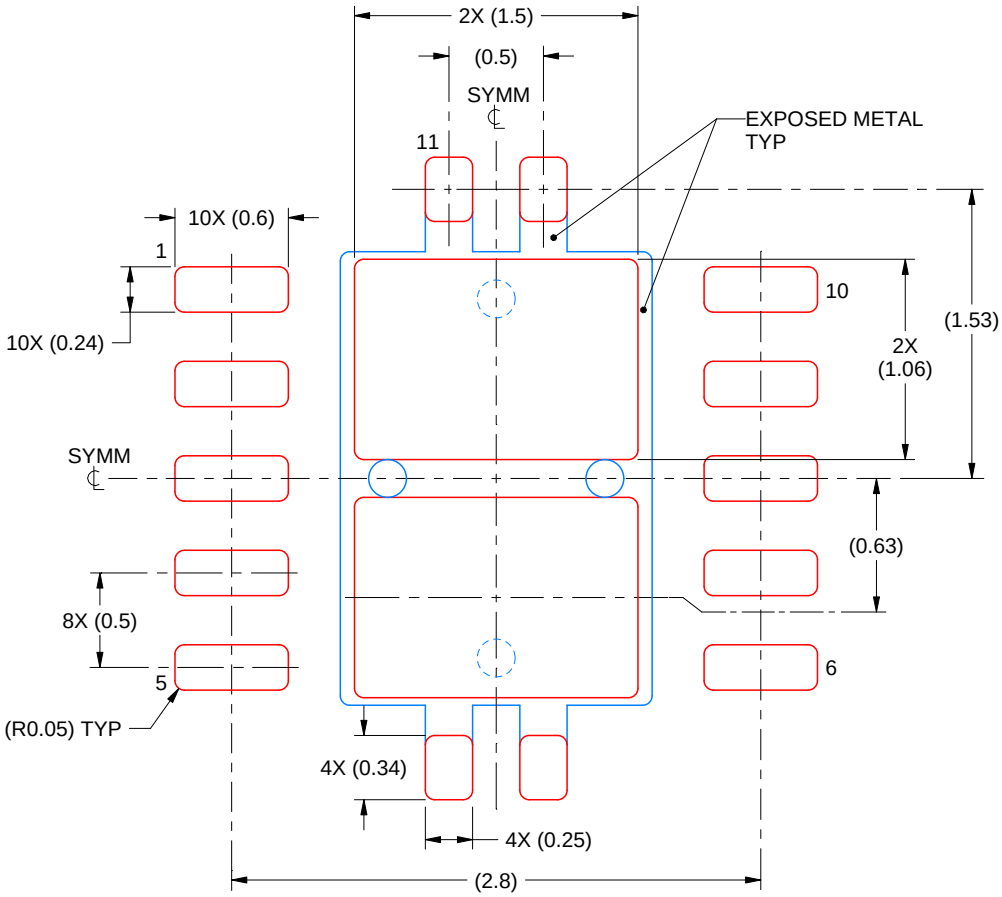
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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