36 – 60V_{IN} ZVS Buck Regulator & LED Driver

Product Description

The PI354x-00 is a family of high input voltage, wide input range DC-DC ZVS Buck regulators integrating controller, power switches, and support components all within a high-density System-in-Package (SiP). The PI354x-00 products are designed to operate within an SELV compliant system with steady state operation limited to 60V. The PI354x-00 products allow for transient voltage conditions up to 70V before shut down is triggered. The integration of a high-performance Zero-Voltage Switching (ZVS) topology, within the PI354x-00 series, increases point of load performance providing best in class power efficiency. The PI354x-00 requires only an external inductor, two voltage selection resistors and minimal capacitors to form a complete DC-DC switching mode buck regulator.

Device	Output Voltage		I_{OUT} Max
	Set	Range	
PI3542-00-xGIZ	2.5V	2.2 – 3.0V	10A
PI3543-00-xGIZ	3.3V	2.6 – 3.6V	10A
PI3545-00-xGIZ	5.0V	4.0 – 5.5V	10A
PI3546-00-xGIZ	12V	6.5 – 14V	9A

PI354x-00 Family can operate in constant voltage output for typical buck regulation applications in addition to constant current output for LED lighting and battery charging applications.

Features & Benefits

- High-Efficiency HV ZVS Buck Topology
- Wide input voltage range of 36 – 60V
- Tolerant of transient events up to 70V_{IN}
- Constant voltage or constant current operation
- Constant current error amplifier and reference
- Power-up into pre-biased load
- Parallel capable up to 3 regulators
- Two-phase interleaving
- Input Over/Undervoltage Lockout (OVLO/UVLO)
- Output Overvoltage Protection (OVP)
- Overtemperature Protection (OTP)
- Fast and slow current limits
- Differential amplifier for output remote sensing
- User adjustable soft-start & tracking
- –40 to 125°C operating range (T_J)

Applications

- HV to PoL Buck Regulator Applications
- Computing, Communications, Industrial, Automotive Accessories
- Constant Current Output Operation:
  - LED Lighting
  - Battery Charging

Package Information

- 10 x 10 x 2.6mm LGA SiP
- 10.5 x 10.5 x 3.05mm BGA SiP

Note: Product images may not highlight current product markings.

Contents

Order Information

Part Number	Output Range		I_{OUT} Max	Package	Transport Media
	Set	Range			
PI3542-00-LGIZ	2.5V	2.2 – 3.0V	10A	10 x 10mm LGA	TRAY
PI3542-00-BGIZ	2.5V	2.2 – 3.0V	10A	10.5 x 10.5mm BGA	TRAY
PI3543-00-LGIZ	3.3V	2.6 – 3.6V	10A	10 x 10mm LGA	TRAY
PI3543-00-BGIZ	3.3V	2.6 – 3.6V	10A	10.5 x 10.5mm BGA	TRAY
PI3545-00-LGIZ	5.0V	4.0 – 5.5V	10A	10 x 10mm LGA	TRAY
PI3545-00-BGIZ	5.0V	4.0 – 5.5V	10A	10.5 x 10.5mm BGA	TRAY
PI3546-00-LGIZ	12V	6.5 – 14V	9A	10 x 10mm LGA	TRAY
PI3546-00-BGIZ	12V	6.5 – 14V	9A	10.5 x 10.5mm BGA	TRAY

Thermal, Storage and Handling Information

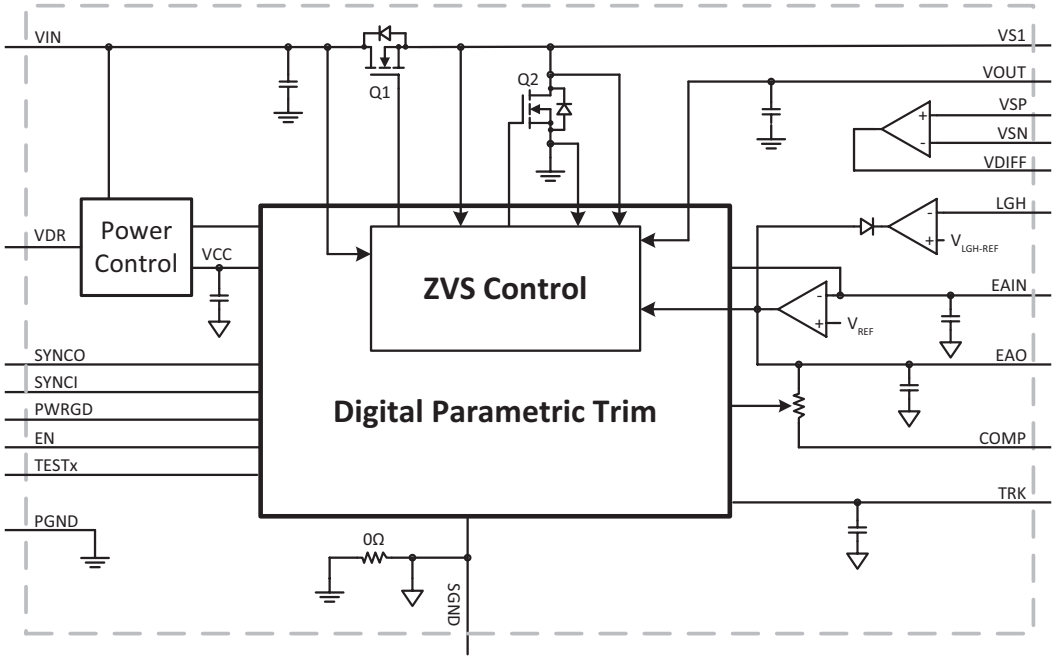
Name	Rating
Storage Temperature	–65°C to 150°C
Internal Operating Temperature	–40°C to 125°C
Soldering Temperature for 20 seconds	245°C
MSL Rating	3
ESD Rating	2kV HBM, 1kV CDM

Absolute Maximum Ratings

Name	Rating
V_{IN}	–0.7V to 75V
VS1	$-0.7V_{DC}$ to 75V
V_{OUT}	–0.5V to 25V
SGND	±100mA
TRK	–0.3V to 5.5V / ±30mA
VDR, SYNCI, SYNCO, PWRGD, EN, LGH, COMP, EAO, EAIN, VDIFF, VSN, VSP, TESTx	–0.3V to 5.5V / ±5mA

Notes: Stresses beyond these limits may cause permanent damage to the device. Operation at these conditions or conditions beyond those listed in the Electrical Specifications table is not guaranteed. All voltage nodes are referenced to PGND unless otherwise noted.

Functional Block Diagram

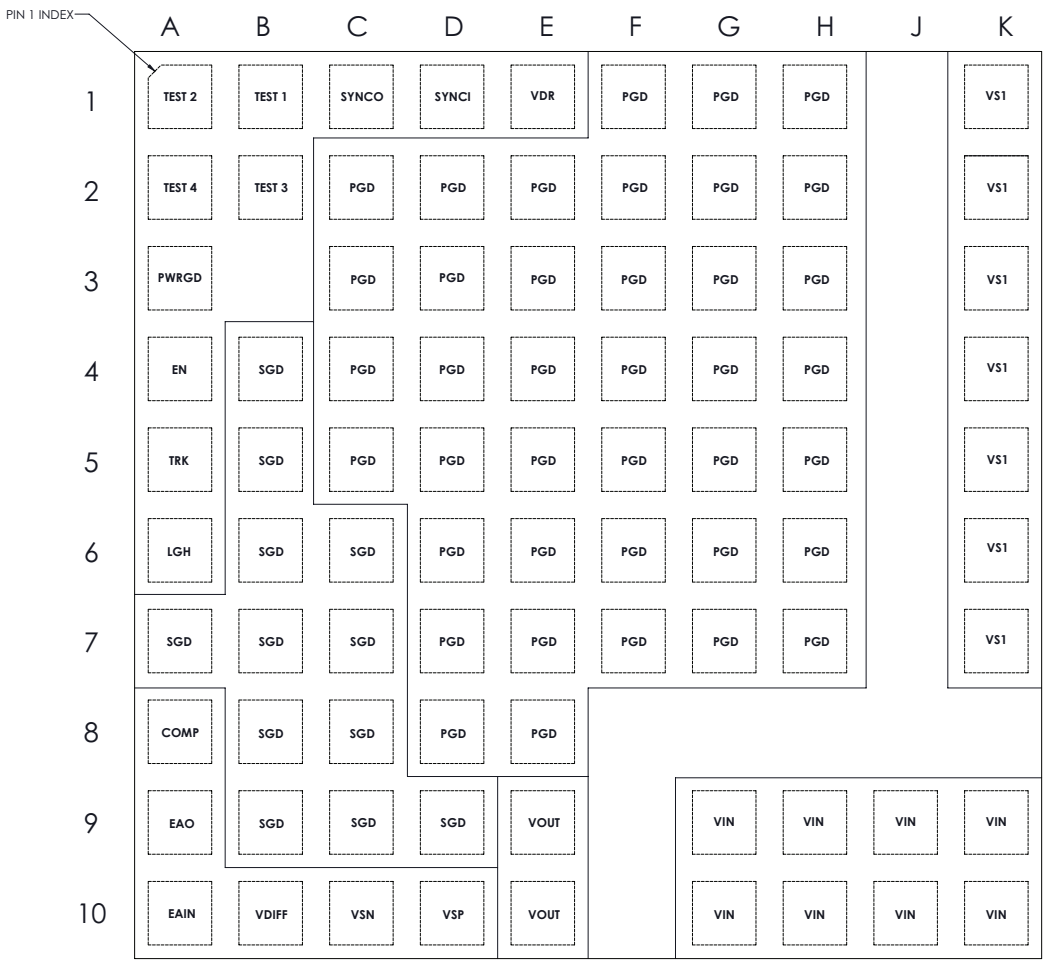


Simplified block diagram

Pin Description

Name	Location	I/O	Description
VS1	Block 2 (See Pkg Pin-Out dwg)	Power	**Switching node:** and ZVS sense for power switches.
VIN	Block 1	Power	**Input voltage:** and sense for UVLO, OVLO and feed forward ramp.
VDR	1E	I/O	**Gate Driver V_{CC} :** Internally generated 5.1V. May be used as reference or low-power bias supply for external loads. See Application Description for Important considerations.
SYNCI	1D	I	**Synchronization input:** Synchronize to the falling edge of external clock frequency. SYNCI is a high-impedance digital input node and should always be connected to SGND when not in use.
SYNCO	1C	O	**Synchronization output:** Outputs a high signal for ½ of the minimum period for synchronization of other regulators.
TESTx	1B, 1A, 2B, 2A	I/O	**Test Connections:** Use only with factory guidance. Connect to SGND for proper operation.
PWRGD	3A	O	**Power Good:** High impedance when regulator is operating and V_{OUT} is in regulation. Otherwise pulls to SGND.
EN	4A	I	**Enable Input:** Regulator enable control. When asserted active or left floating: regulator is enabled. Otherwise regulator is disabled.
TRK	5A	I	**Soft-start and track input:** An external capacitor may be connected between TRK pin and SGND to decrease the rate of rise during soft-start.
LGH	6A	I	**Lighting (LGH)/Constant Current (CC) Sense Input:** Input with a 100mV threshold. Used for lighting and constant current type applications.When not using the constant current mode (CC mode), the LGH pin should be connected to SGND.
COMP	8A	O	**Compensation Capacitor:** Connect capacitor for control loop dominant pole. See Error Amplifier section for details. A default CCOMP of 4.7nF is used in the example
EAO	9A	O	**Error amp output:** External connection for additional compensation and current sharing.
EAIN	10A	I	**Error Amp Inverting Input:** Connection for the feedback divider tap.
VDIFF	10B	O	**Independent Amplifier Output:** Active only when module is enabled.
VSN	10C	I	**Independent Amplifier Inverting Input:** If unused, connect in unity gain
VSP	10D	I	**Independent Amplifier Non-Inverting Input:** If unused, connect in SGND
VOUT	9E, 10E	Power	**Direct VOUT Connect:** for per-cycle internal clamp node and feed-forward ramp.
SGND	Block 4	-	**Signal ground:** Internal logic ground for EA, TRK, SYNCI, SYNCO communication returns. SGND and PGND are star connected within the regulator package.
PGND	Block 3	Power	**Power ground:** V_{IN} and V_{OUT} power returns.

Package Pinout



TOP THROUGH VIEW OF PRODUCT
PI354X

Large Pin Blocks

Pin Block Name	Group of pins
VIN	K9-10, J9-10, H9-10, G9-10
VS1	K1-7
PGND	H1-7, G1-7,F1-7, E2-8, D2-8, C2-5
SGND	D9, C6-9, B4-9, A7

PI354x-00 Common Electrical Characteristics

Specifications apply for –40°C < T_J < 125°C, V_{IN} = 48V, EN = High, V_{VDR} = 5.1V ±2%, L1 = 340nH [a] unless other conditions are noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Differential Amp						
Open Loop Gain			96	120	140	dB
Small Signal Gain-Bandwidth			5	7	12	MHz
Offset			–1	0.5	1	mV
Common Mode Input Range			–0.1		2.5	V
Differential Mode Input Range					2	V
Input Bias Current			–1		1	µA
Maximum V_{OUT}		I_{DIFF} = –1mA	V_{VDR} – 0.2			V
Minimum V_{OUT}					20	mV
Capacitive Load Range for Stability			0		50	pF
Slew Rate Rising				11		V/µs
Slew Rate Falling				11		V/µs
Sink/Source Current			–1		1	mA
Current Source Function (LGH)						
LGH Reference	$V_{LGH-REF}$		95	100	107	mV
Input Offset				0.5		mV
Gain-Bandwidth Product			3			MHz
Internal Feedback Capacitance				20		pF
Gain				10		V/V
Intermediate Reference				1		V
Transconductance				1		mS
Output Current Capability		Sink current only	1			mA
PWRGD						
PWRGD Rising Threshold	$V_{PG\_HI\%}$	[b]	79	85	91	% V_{OUT_DC}
PWRGD Falling Threshold	$V_{PG\_LO\%}$	[b]	77	83	89	% V_{OUT_DC}
PWRGD Output Low	V_{PG_SAT}	Sink = 4mA [b]			0.4	V
PWRGD Sink Current	I_{PG_SAT}	[b]		4		mA

[a] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI354x evaluation board with 2.5 x 4in dimensions and 4-layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[b] Regulator is assured to meet performance specifications by design, test correlation, characterization and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[c] Output current capability may be limited and other performance may vary from noted electrical characteristics when V_{OUT} is not set to nominal.
[d] Refer to output ripple plots.
[e] Refer to Load current vs. ambient temperature curves.
[f] Refer to switching frequency vs. load current curves.

PI354x-00 Common Electrical Characteristics (Cont.)

Specifications apply for –40°C < T_J < 125°C, V_{IN} = 48V, EN = High, V_{VDR} = 5.1V ±2%, L1 = 340nH [a] unless other conditions are noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Enable						
High Threshold	V_{EN_HI}		0.9	1	1.1	V
Low Threshold	V_{EN_LO}		0.7	0.8	0.9	V
Threshold Hysteresis	V_{EN_HYS}		100	200	300	mV
Enable Pull-Up Voltage	V_{EN_PU}			2		V
Source Current	I_{EN_SO}			50		µA
VDR						
Voltage Setpoint	V_{VDR}	V_{IN_DC} > 10V	4.8	5.1	5.4	V
External Loading	I_{VDR}	See Application Description for details	0		2	mA
Protection						
Input UVLO Start Threshold	V_{UVLO_START}		33.8	34.8	35.8	V
Input UVLO Stop Hysteresis	V_{UVLO_HYS}			2.5		V
Input UVLO Response Time				1.25		us
Input OVLO Stop Threshold	V_{OVLO}		70			V
Input OVLO Start Hysteresis	V_{OVLO_HYS}			1.3		V
Input OVLO Response Time	t_f			1.25		µs
Output Overvoltage Protection	V_{OVP}	Above set V_{OUT}		20		%
Sync In (SYNCI)						
Synchronization Frequency Range	Δf_{SYNCI}	Relative to set switching frequency [c]	50		110	%
SYNCI Threshold	V_{SYNCI}			V_{VDR} / 2		V
Sync Out (SYNCO)						
SYNCO High	V_{SYNCO_HI}	Source 1mA	V_{VDR} –0.5			V
SYNCO Low	V_{SYNCO_LO}	Sink 1mA			0.5	V
SYNCO Rise Time	t_{SYNCO_RT}	20pF load		10		ns
SYNCO Fall Time	t_{SYNCO_FT}	20pF load		10		ns

[a] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI354x evaluation board with 2.5 x 4in dimensions and 4-layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[b] Regulator is assured to meet performance specifications by design, test correlation, characterization and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[c] Output current capability may be limited and other performance may vary from noted electrical characteristics when V_{OUT} is not set to nominal.
[d] Refer to output ripple plots.
[e] Refer to load current vs. ambient temperature curves.
[f] Refer to switching frequency vs. load current curves.

PI3542-00 ($2.5V_{OUT}$) Electrical Characteristics

Specifications apply for –40°C < T_J < 125°C, V_{IN} = 48V, EN = High, V_{VDR} = 5.1V ±2%, L1 = 340nH [a] unless other conditions are noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Specifications						
Input Voltage	V_{IN_DC}		36	48	60	V
Input Voltage, Transient	V_{IN_TRANS}	< 1% duty cycle,entire transient duration < 10ms			70	V
Input Current	I_{IN_DC}	V_{IN} = 48V, T_C = 25°C, I_{OUT} = 10A		0.597		A
Input Current At Output Short (Fault Condition Duty Cycle)	I_{IN_Short}	Short at terminals		3.1		mA
Input Quiescent Current	I_{Q_VIN}	Disabled		0.75		mA
		Enabled (no load)		1.4		
Input Voltage Slew Rate	V_{IN_SR}				1	V/µs
Output Specifications						
EAIN Voltage Total Regulation	V_{EAIN}	[b]	0.985	1.00	1.015	V
Output Voltage Trim Range	V_{OUT_DC}	[b] [c]	2.2	2.5	3.0	V
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	@ 25°C, 36V < V_{IN} < 60V		0.10		%
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	@ 25°C, 0.5A < I_{OUT} < 10A		0.10		%
Output Voltage Ripple	V_{OUT_AC}	I_{OUT} = 10A, C_{OUT} = 6 x 100µF, 20MHz BW [d]		47		mVp-p
Output Current	I_{OUT_DC}	[e]	0		10	A
Maximum Array Size	$N_{Parallel}$				3	Modules
Output Current, Array of 2	$I_{OUT\_DC\text{-}ARRAY2}$	Total array capability, see applications section for details	0		17.7	A
Output Current, Array of 3	$I_{OUT\_DC\text{-}ARRAY2}$	Total array capability, see applications section for details	0		25.4	A
Current Limit	I_{OUT_CL}	Typ limit based on nominal 340nH inductor.		12		A
Timing						
Switching Frequency	f_S	[f] 48V_{IN} to 2.5V_{OUT}, 3A out, L1 = 340nH ±1%	-	400	-	kHz
Fault Restart Delay	t_{FR_DLY}			30		ms

[a] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI354x evaluation board with 2.5 x 4in dimensions and 4-layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[b] Regulator is assured to meet performance specifications by design, test correlation, characterization and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[c] Output current capability may be limited and other performance may vary from noted electrical characteristics when V_{OUT} is not set to nominal.
[d] Refer to output ripple plots.
[e] Refer to load current vs. ambient temperature curves.
[f] Refer to switching frequency vs. load current curves.

PI3542-00 ($2.5V_{OUT}$) Electrical Characteristics (Cont.)

Specifications apply for –40°C < T_J < 125°C, V_{IN} = 48V, EN = High, V_{VDR} = 5.1V ±2%, L1 = 340nH [a] unless other conditions are noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Soft Start, Tracking and Error Amplifier						
TRK Active Range (Nominal)	V_{TRK}		0		1.4	V
TRK Enable Threshold	V_{TRK_OV}		20	40	60	mV
TRK to EAIN Offset	V_{EIAN_OV}	V_{TRK} = 0.5V, EAO shorted to EAIN	50	80	110	mV
Charge Current (Soft-Start)	I_{TRK}		70	50	30	µA
Discharge Current (Fault)	I_{TRK_DIS}	V_{TRK} = 0.5V		10		mA
Soft-Start Time	t_{SS}	C_{TRK} = 0µF	0.6	0.94	1.6	ms
Error Amplifier Trans-Conductance	GM_{EAO}	[b]		5.1		mS
PSM Skip Threshold	PSM_{SKIP}	[b]		0.8		V
Error Amplifier Output Impedance	R_{OUT}	[b]	1			MΩ
Internal Compensation Capacitor	C_{HF}	[b]		56		pf
Internal Compensation Resistor	R_{ZI}	[b]		5		kΩ

[a] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI354x evaluation board with 2.5 x 4in dimensions and 4-layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[b] Regulator is assured to meet performance specifications by design, test correlation, characterization and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[c] Output current capability may be limited and other performance may vary from noted electrical characteristics when V_{OUT} is not set to nominal.
[d] Refer to output ripple plots.
[e] Refer to load current vs. ambient temperature curves.
[f] Refer to switching frequency vs. load current curves.

PI3542-00 (2.5V_{OUT}) Electrical Characteristics (Cont.)

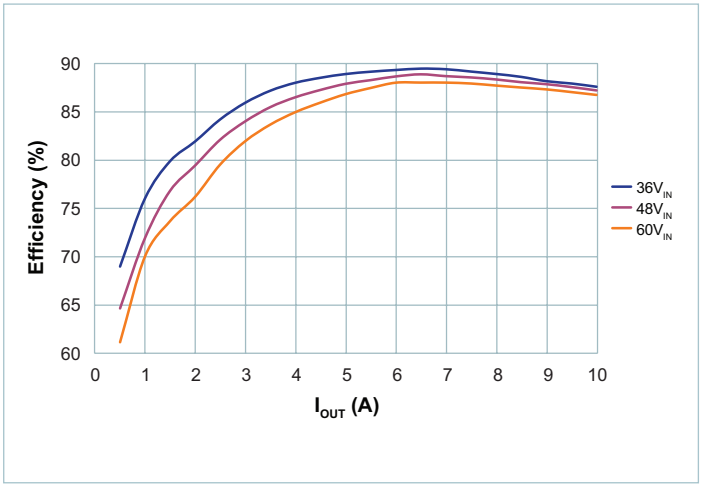


Figure 1 *— Regulator efficiency*

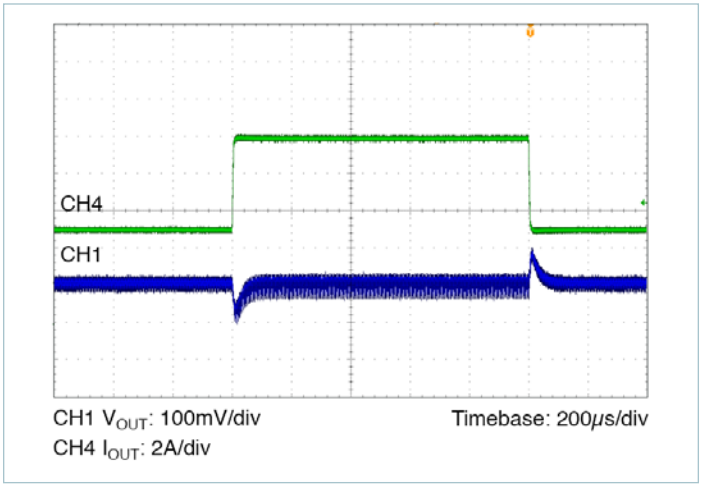


Figure 2 *— Transient response: 5A to 10A, at 1A/µs. 48V_{IN} to 2.5V_{OUT}, C_{OUT} = 6 x 100µF ceramic*

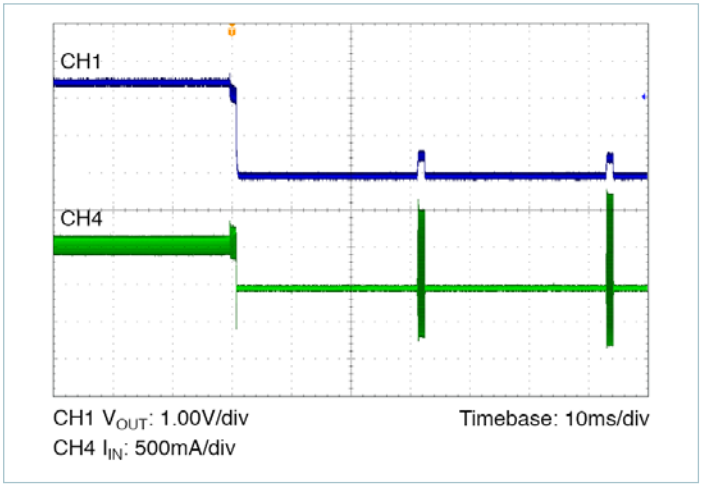


Figure 3 *— Output short circuit @ V_{IN} = 48V*

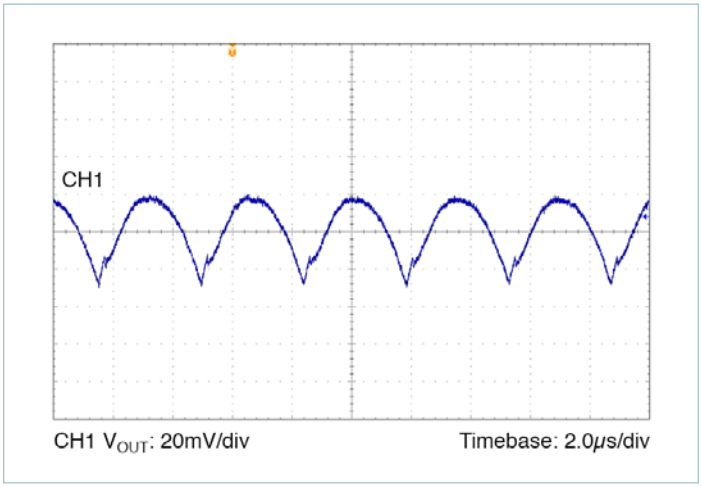


Figure 4 *— Output ripple: 48V_{IN}, 2.5V_{OUT} at 10A. V_{OUT} = 20mV/Div, 2.0µs/Div; C_{OUT} = 6 x 100µF ceramic*

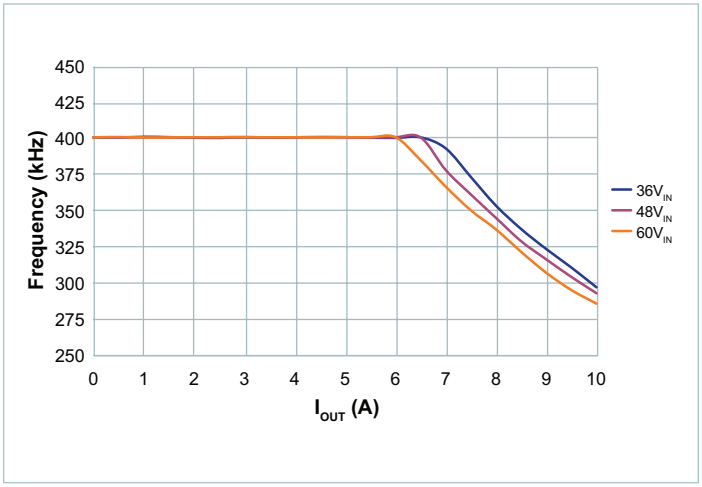


Figure 5 *— Switching frequency vs. load current*

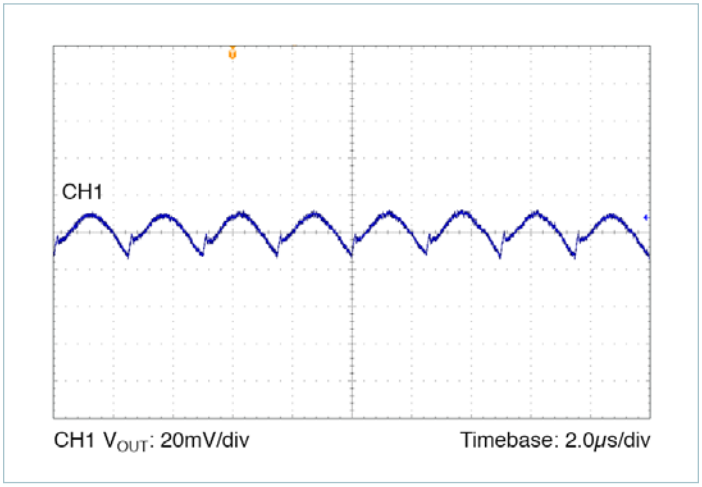


Figure 6 *— Output ripple: 48V_{IN}, 2.5V_{OUT} at 5A. V_{OUT} = 20mV/Div, 2.0µs/Div; C_{OUT} = 6 x 100µF ceramic*

PI3542-00 (2.5V_{OUT}) Electrical Characteristics (Cont.)

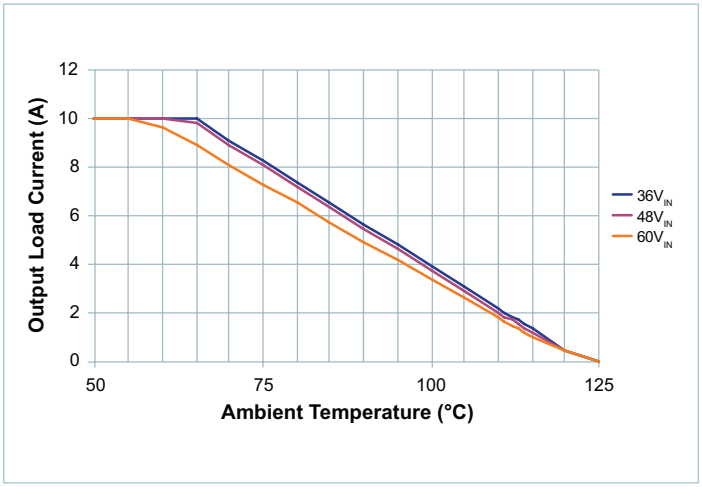


Figure 7 — *Load current vs. ambient temperature, 0LFM*

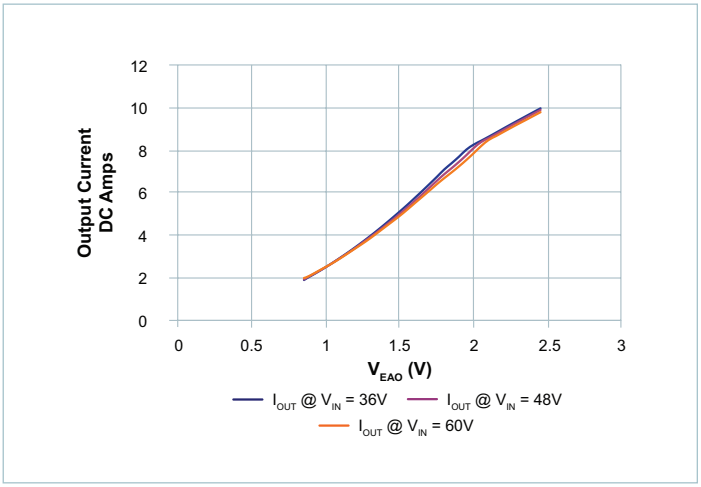


Figure 10 — *Output current vs. error voltage V_{EAO}*

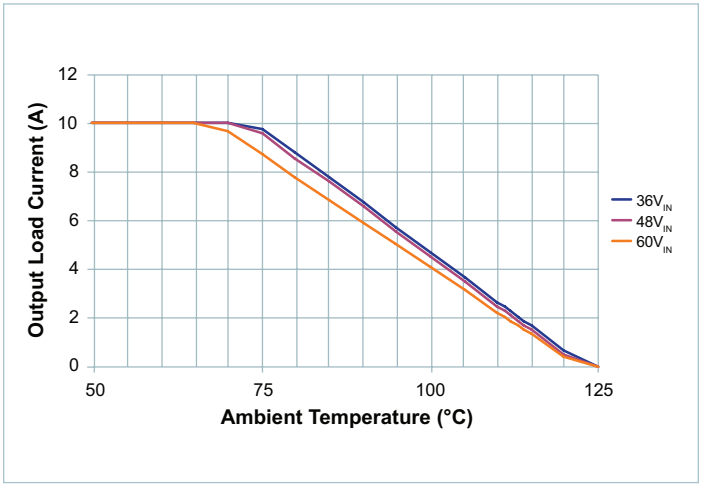


Figure 8 — *Load current vs. ambient temperature, 200LFM*

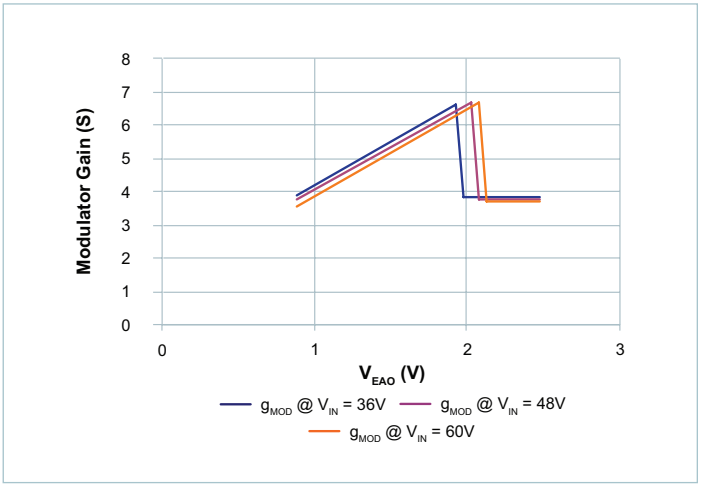


Figure 11 — *Modulator gain vs. error voltage V_{EAO}*

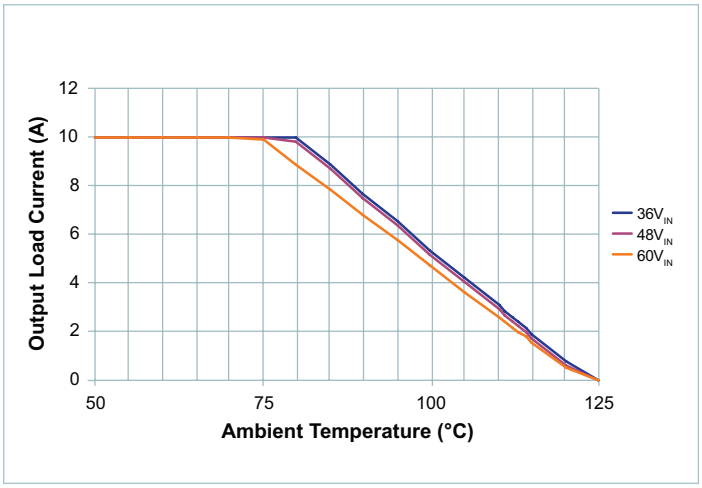


Figure 9 — *Load current vs. ambient temperature, 400LFM*

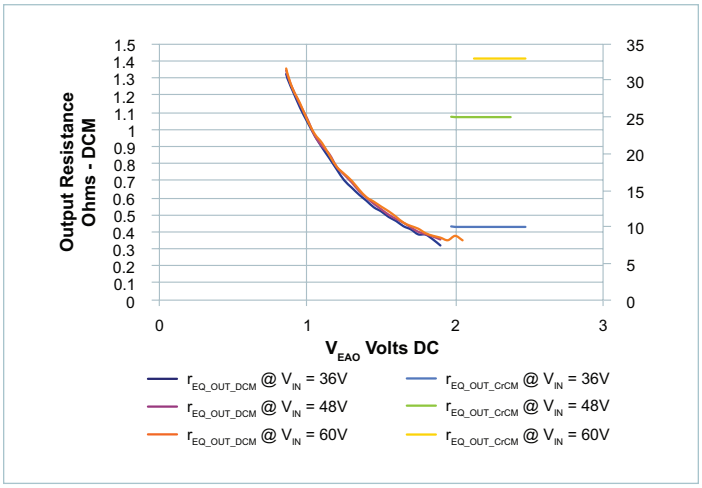


Figure 12 — *Output Equivalent Resistance vs.Error Voltage V_{EAO}*

PI3543-00 ($3.3V_{OUT}$) Electrical Characteristics

Specifications apply for –40°C < T_J < 125°C, V_{IN} = 48V, EN = High, V_{VDR} = 5.1V ±2%, L1 = 420nH [a] unless other conditions are noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Specifications						
Input Voltage	V_{IN_DC}		36	48	60	V
Input Voltage, Transient	V_{IN_TRANS}	< 1% duty cycle,entire transient duration < 10ms			70	V
Input Current	I_{IN_DC}	V_{IN} = 48V, T_C = 25°C, I_{OUT} = 10A		0.762		A
Input Current At Output Short (Fault Condition Duty Cycle)	I_{IN_Short}	Short at terminals		3	-	mA
Input Quiescent Current	I_{Q_VIN}	Disabled		0.75		mA
		Enabled (no load)		1.6		
Input Voltage Slew Rate	V_{IN_SR}				1	V/µs
Output Specifications						
EAIN Voltage Total Regulation	V_{EAIN}	[b]	0.985	1.00	1.015	V
Output Voltage Trim Range	V_{OUT_DC}	[b] [c]	2.6	3.3	3.6	V
Line Regulation	$\Delta V_{OUT} / \Delta V_{IN}$	@ 25°C, 36V < V_{IN} < 60V		0.10		%
Load Regulation	$\Delta V_{OUT} / \Delta I_{OUT}$	@ 25°C, 0.5A < I_{OUT} < 10A		0.10		%
Output Voltage Ripple	V_{OUT_AC}	I_{OUT} = 10A, C_{OUT} = 6 x 100µF, 20MHz BW [d]		62		mVp-p
Output Current	I_{OUT_DC}	[e]	0		10	A
Maximum Array Size	$N_{Parallel}$				3	Modules
Output Current, Array of 2	$I_{OUT\_DC\text{-}ARRAY2}$	Total array capability, see applications section for details	0		17.7	A
Output Current, Array of 3	$I_{OUT\_DC\text{-}ARRAY2}$	Total array capability, see applications section for details	0		25.4	A
Current Limit	I_{OUT_CL}	Typ limit based on nominal 420nH inductor		11.5		A
Timing						
Switching Frequency	f_S	[f] 48V_{IN} to 3.3V_{OUT}, 6A out, L1 = 420nH ±1%	-	400	-	kHz
Fault Restart Delay	t_{FR_DLY}			30		ms

[a] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI354x evaluation board with 2.5 x 4in dimensions and 4-layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[b] Regulator is assured to meet performance specifications by design, test correlation, characterization and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[c] Output current capability may be limited and other performance may vary from noted electrical characteristics when V_{OUT} is not set to nominal.
[d] Refer to output ripple plots.
[e] Refer to load current vs. ambient temperature curves.
[f] Refer to switching frequency vs. load current curves.

PI3543-00 ($3.3V_{OUT}$) Electrical Characteristics (Cont.)

Specifications apply for –40°C < T_J < 125°C, V_{IN} = 48V, EN = High, V_{VDR} = 5.1V ±2%, L1 = 420nH [a] unless other conditions are noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Soft Start, Tracking and Error Amplifier						
TRK Active Range (Nominal)	V_{TRK}		0		1.4	V
TRK Enable Threshold	V_{TRK_OV}		20	40	60	mV
TRK to EAIN Offset	V_{EIAN_OV}	V_{TRK} = 0.5V, EAO shorted to EAIN	50	80	110	mV
Charge Current (Soft-Start)	I_{TRK}		70	50	30	µA
Discharge Current (Fault)	I_{TRK_DIS}	V_{TRK} = 0.5V		10		mA
Soft-Start Time	t_{SS}	C_{TRK} = 0µF	0.6	0.94	1.6	ms
Error Amplifier Trans-Conductance	GM_{EAO}	[b]		5.1		mS
PSM Skip Threshold	PSM_{SKIP}	[b]		0.8		V
Error Amplifier Output Impedance	R_{OUT}	[b]	1			MΩ
Internal Compensation Capacitor	C_{HF}	[b]		56		pf
Internal Compensation Resistor	R_{ZI}	[b]		6		kΩ

[a] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI354x evaluation board with 2.5 x 4in dimensions and 4-layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[b] Regulator is assured to meet performance specifications by design, test correlation, characterization and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[c] Output current capability may be limited and other performance may vary from noted electrical characteristics when V_{OUT} is not set to nominal.
[d] Refer to output ripple plots.
[e] Refer to load current vs. ambient temperature curves.
[f] Refer to switching frequency vs. load current curves.

PI3543-00 (3.3V_{OUT}) Electrical Characteristics (Cont.)

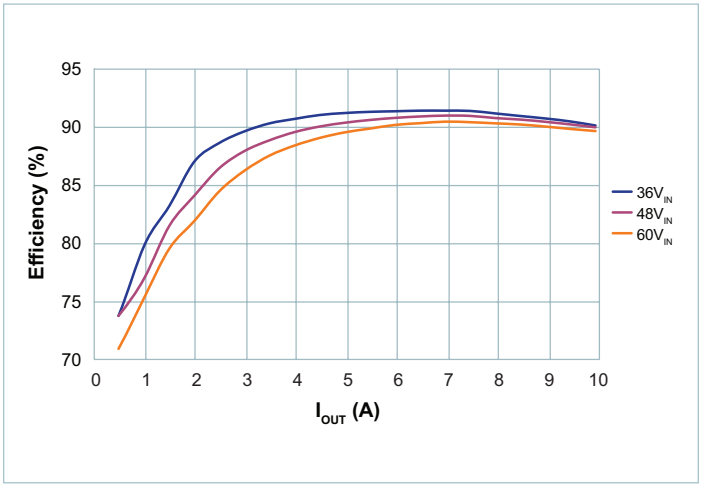


Figure 13 — *Regulator efficiency*

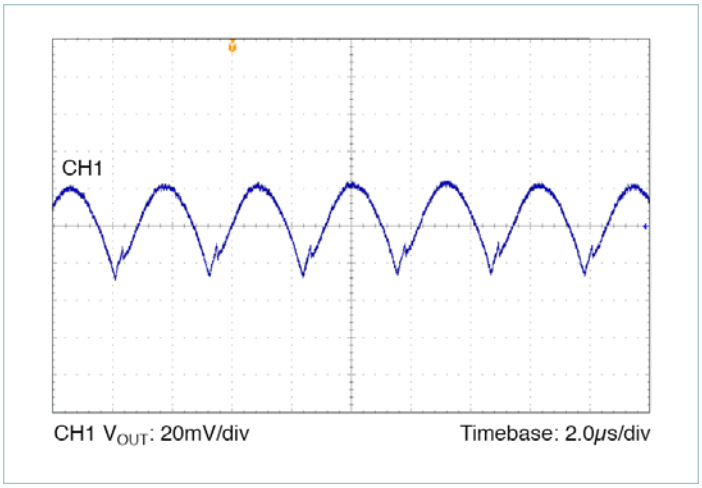


Figure 16 — *Output ripple: 48V_{IN}, 3.3V_{OUT} at 10A.*
V_{OUT} = 20mV/Div, 2.0µs/Div;
C_{OUT} = 6 x 100µF ceramic

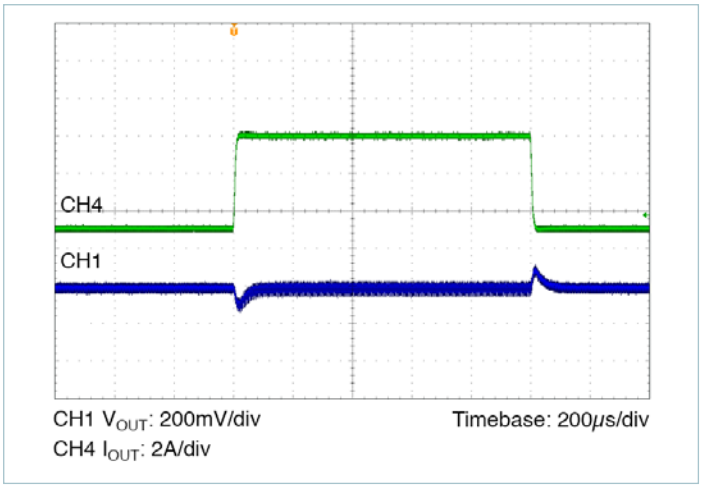


Figure 14 — *Transient response: 5A to 10A, at 1A/µs. 48V_{IN} to 3.3V_{OUT}, C_{OUT} = 6 x 100µF ceramic*

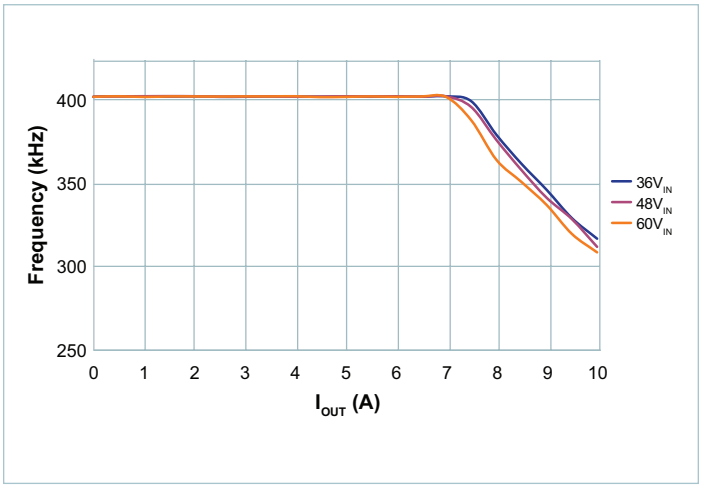


Figure 17 — *Switching frequency vs. load current*

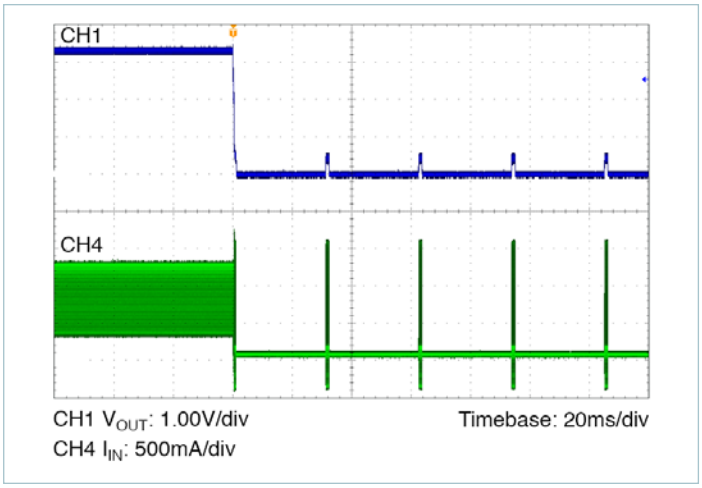


Figure 15 — *Output short circuit @ V_{IN} = 48V*

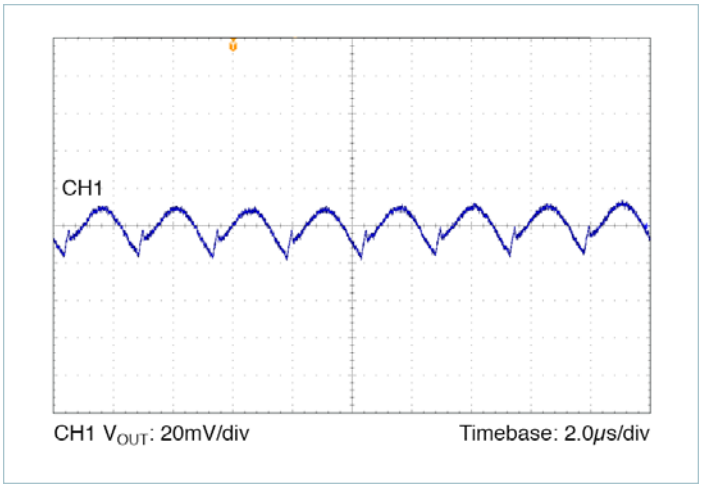


Figure 18 — *Output ripple: 48V_{IN}, 3.3V_{OUT} at 5A.*
V_{OUT} = 20mV/Div, 2.0µs/Div;
C_{OUT} = 6 x 100µF ceramic

PI3543-00 ($3.3V_{OUT}$) Electrical Characteristics (Cont.)

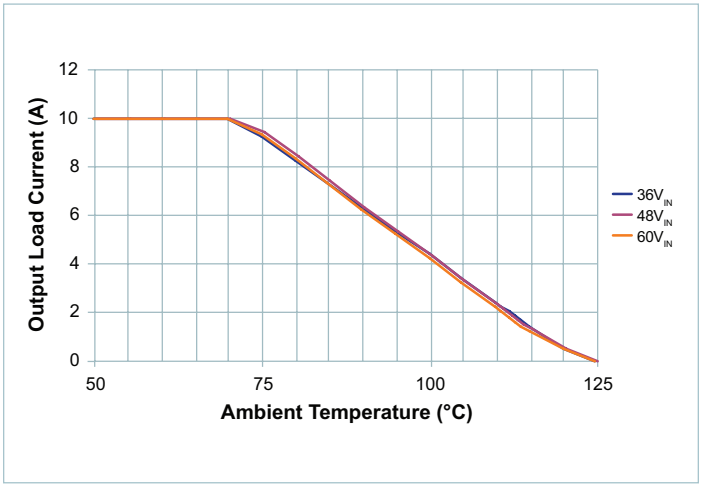


Figure 19 — *Load current vs. ambient temperature, 0LFM*

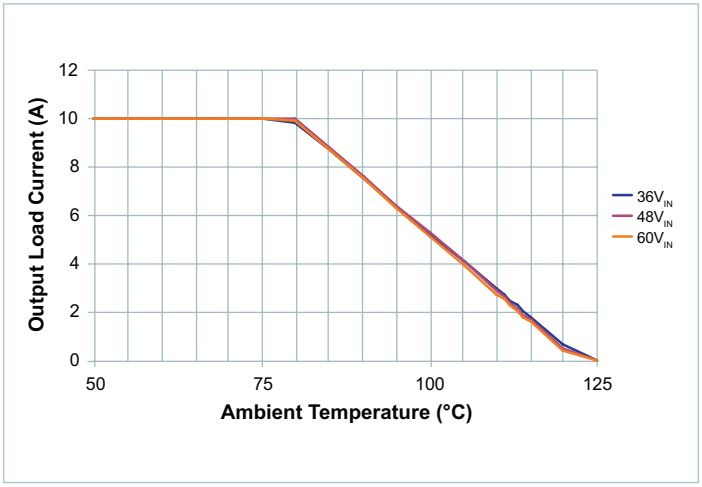


Figure 20 — *Load current vs. ambient temperature, 200LFM*

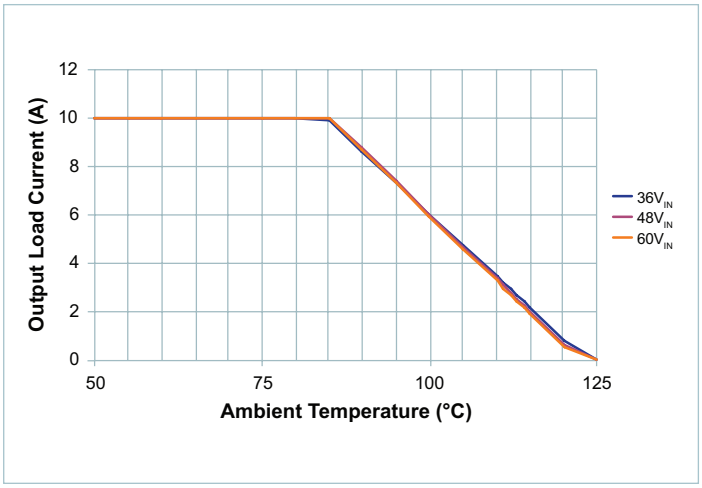


Figure 21 — *Load current vs. ambient temperature, 400LFM*

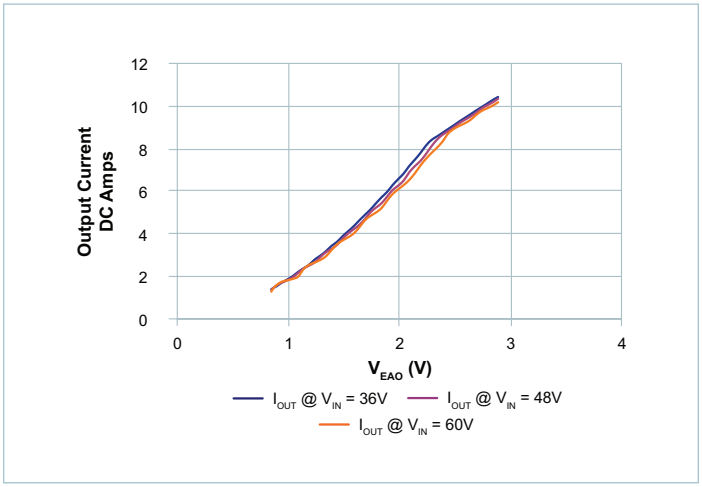


Figure 22 — *Output current vs. error voltage V_{EAO}*

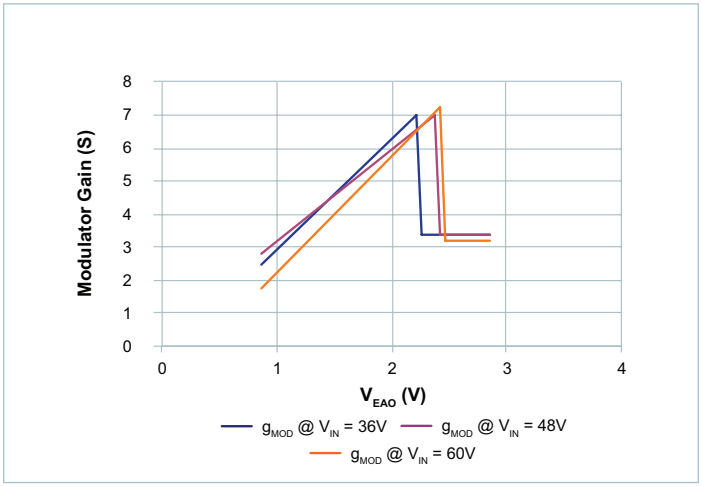


Figure 23 — *Modulator gain vs. error voltage V_{EAO}*

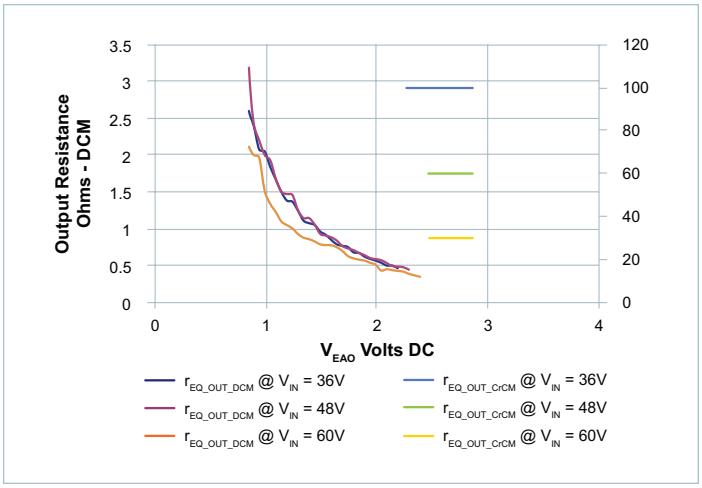


Figure 24 — *Output equivalent resistance vs. error voltage V_{EAO}*

PI3545-00 (5.0V_{OUT}) Electrical Characteristics

Specifications apply for –40°C < T_J < 125°C, V_{IN} = 48V, EN = High, V_{VDR} = 5.1V ±2%, L1 = 420nH [a] unless other conditions are noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Specifications						
Input Voltage	V_{IN_DC}		36	48	60	V
Input Voltage, Transient	V_{IN_TRANS}	< 1% duty cycle,entire transient duration < 10ms			70	V
Input Current	I_{IN_DC}	V_{IN} = 48V, T_C = 25°C, I_{OUT} = 10A		1.126		A
Input Current At Output Short (Fault Condition Duty Cycle)	I_{IN_Short}	Short at terminals		3.2	-	mA
Input Quiescent Current	I_{Q_VIN}	Disabled		0.75		mA
		Enabled (no load)		1.8		
Input Voltage Slew Rate	V_{IN_SR}				1	V/µs
Output Specifications						
EAIN Voltage Total Regulation	V_{EAIN}	[b]	0.985	1.00	1.015	V
Output Voltage Trim Range	V_{OUT_DC}	[b] [c]	4.0	5.0	5.5	V
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	@ 25°C, 36V < V_{IN} < 60V		0.10		%
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	@ 25°C, 0.5A < I_{OUT} < 10A		0.10		%
Output Voltage Ripple	V_{OUT_AC}	I_{OUT} = 10A, C_{OUT} = 6 x 47µF, 20MHz BW [d]		62.4		mVp-p
Output Current	I_{OUT_DC}	[e]	0		10	A
Maximum Array Size	$N_{Parallel}$				3	Modules
Output Current, Array of 2	$I_{OUT\_DC\text{-}ARRAY2}$	Total array capability, see applications section for details	0		17.7	A
Output Current, Array of 3	$I_{OUT\_DC\text{-}ARRAY2}$	Total array capability, see applications section for details	0		25.4	A
Current Limit	I_{OUT_CL}	Typ limit based on nominal 420nH inductor.		12		A
Timing						
Switching Frequency	f_S	[f] 48V_{IN} to 5V_{OUT}, 3A out, L1 = 420nH ±1%	-	600	-	kHz
Fault Restart Delay	t_{FR_DLY}			30		ms

[a] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI354x evaluation board with 2.5 x 4in dimensions and 4-layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[b] Regulator is assured to meet performance specifications by design, test correlation, characterization and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[c] Output current capability may be limited and other performance may vary from noted electrical characteristics when V_{OUT} is not set to nominal.
[d] Refer to output ripple plots.
[e] Refer to load current vs. ambient temperature curves.
[f] Refer to switching frequency vs. load current curves.

PI3545-00 ($5.0V_{OUT}$) Electrical Characteristics (Cont.)

Specifications apply for –40°C < T_J < 125°C, V_{IN} = 48V, EN = High, V_{VDR} = 5.1V ±2%, L1 = 420nH [a] unless other conditions are noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Soft Start, Tracking and Error Amplifier						
TRK Active Range (Nominal)	V_{TRK}		0		1.4	V
TRK Enable Threshold	V_{TRK_OV}		20	40	60	mV
TRK to EAIN Offset	V_{EIAN_OV}	V_{TRK} = 0.5V, EA0 shorted to EAIN	50	80	110	mV
Charge Current (Soft-Start)	I_{TRK}		70	50	30	µA
Discharge Current (Fault)	I_{TRK_DIS}	V_{TRK} = 0.5V		10		mA
Soft-Start Time	t_{SS}	C_{TRK} = 0µF	0.6	0.94	1.6	ms
Error Amplifier Trans-Conductance	GM_{EAO}	[b]		5.1		mS
PSM Skip Threshold	PSM_{SKIP}	[b]		0.8		V
Error Amplifier Output Impedance	R_{OUT}	[b]	1			MΩ
Internal Compensation Capacitor	C_{HF}	[b]		56		pf
Internal Compensation Resistor	R_{ZI}	[b]		6		kΩ

[a] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI354x evaluation board with 2.5 x 4in dimensions and 4-layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[b] Regulator is assured to meet performance specifications by design, test correlation, characterization and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[c] Output current capability may be limited and other performance may vary from noted electrical characteristics when V_{OUT} is not set to nominal.
[d] Refer to output ripple plots.
[e] Refer to load current vs. ambient temperature curves.
[f] Refer to switching frequency vs. load current curves.

PI3545-00 ($5.0V_{OUT}$) Electrical Characteristics (Cont.)

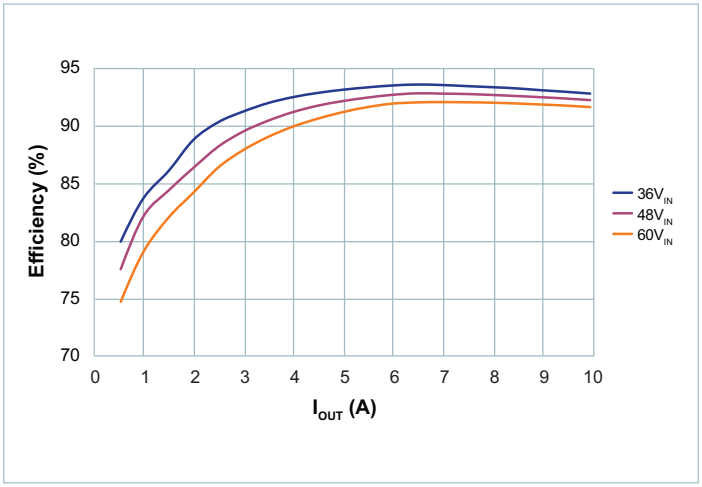


Figure 25 — *Regulator efficiency at 25°C*

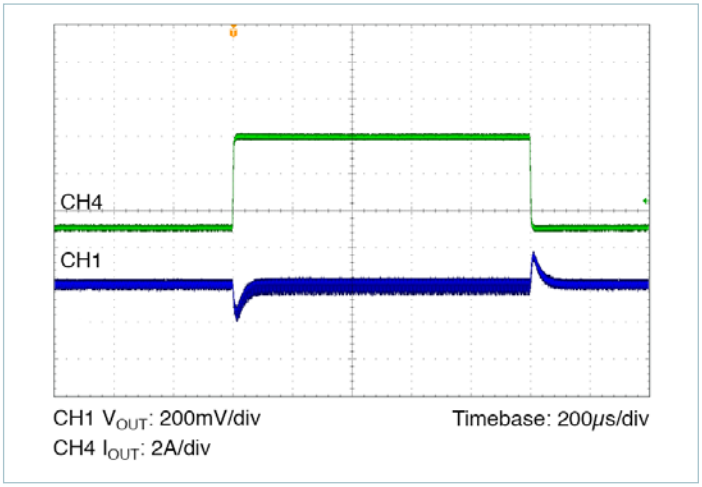


Figure 26 — *Transient response: 5A to 10A, at 1A/µs. $48V_{IN}$ to $5.0V_{OUT}$ C_{OUT} = 6 x 47µF ceramic*

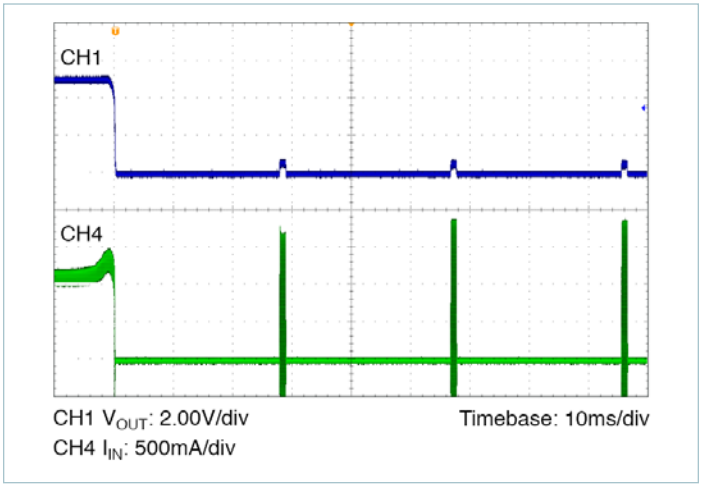


Figure 27 — *Output short circuit @ V_{IN} = 48V*

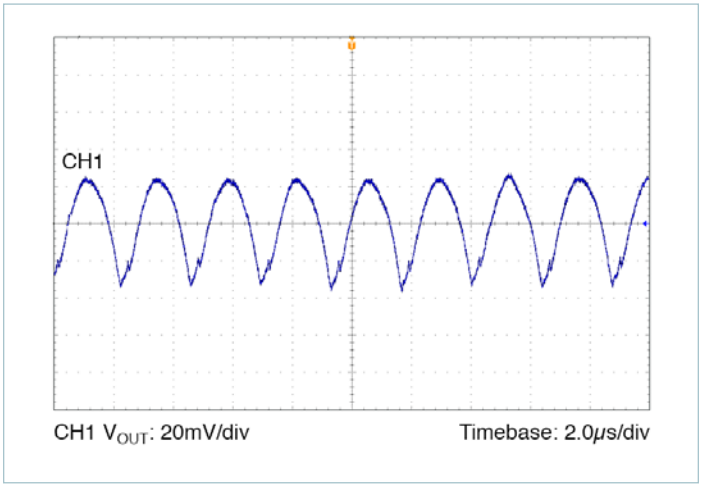


Figure 28 — *Output ripple: $48V_{IN}$, $5.0V_{OUT}$ at 10A.*
V_{OUT} = 20mV/Div, 2.0µs/Div;
C_{OUT} = 6 x 47µF ceramic

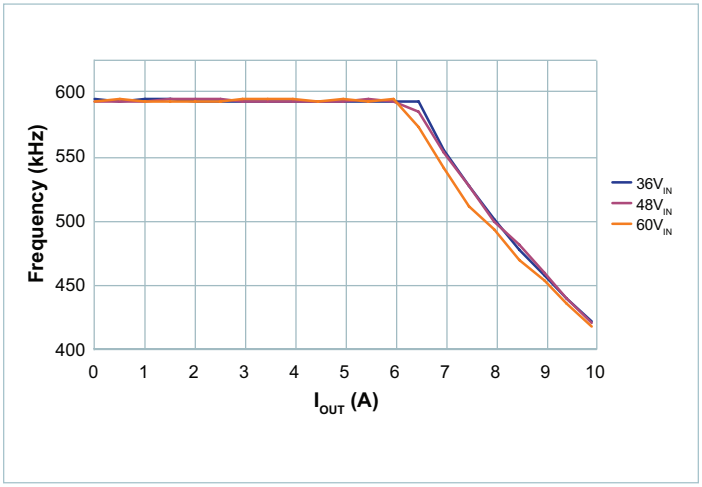


Figure 29 — *Switching frequency vs. load current*

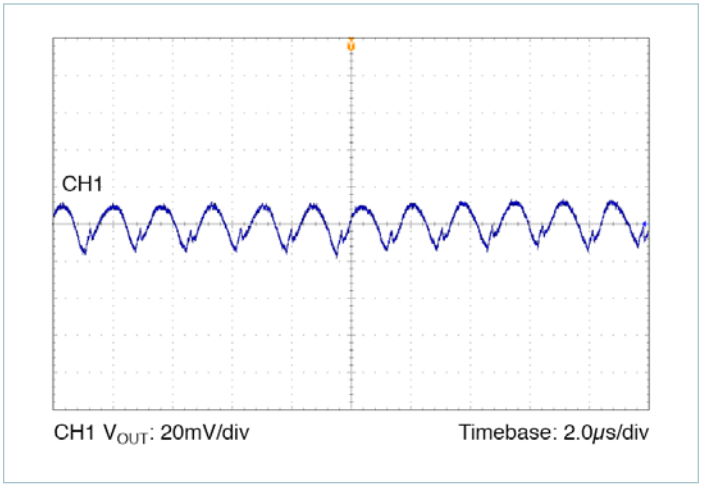


Figure 30 — *Output ripple: $48V_{IN}$, $5.0V_{OUT}$ at 5A.*
V_{OUT} = 20mV/Div, 2.0µs/Div;
C_{OUT} = 6 x 47µF ceramic

PI3545-00 (5.0V_{OUT}) Electrical Characteristics (Cont.)

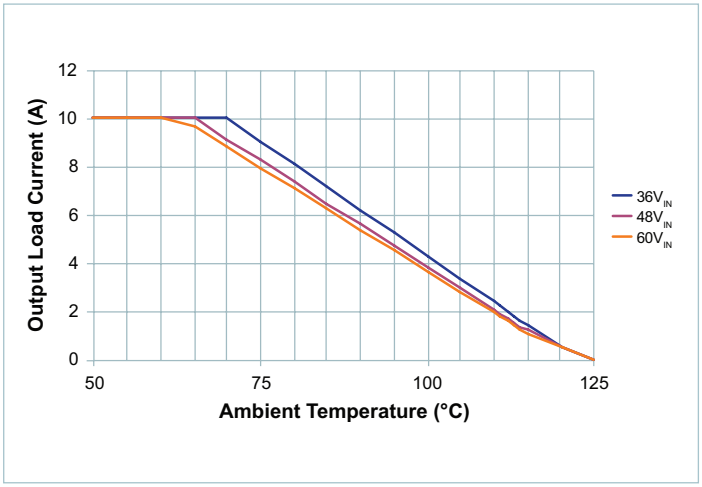


Figure 31 — *Load current vs. ambient temperature, 0LFM*

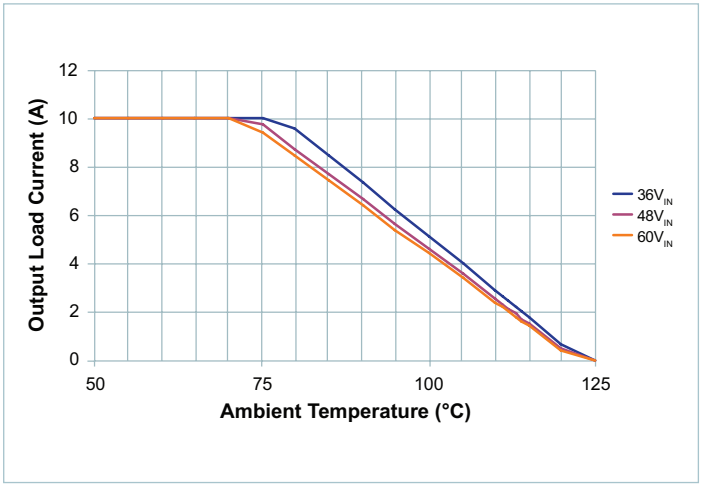


Figure 32 — *Load current vs. ambient temperature, 200LFM*

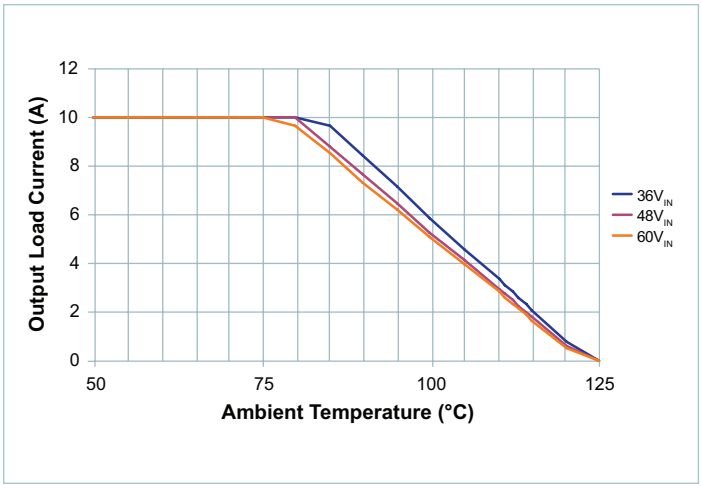


Figure 33 — *Load current vs. ambient temperature, 400LFM*

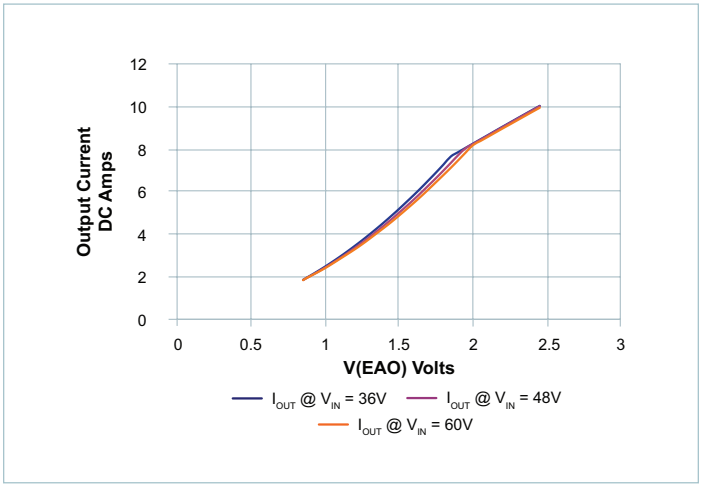


Figure 34 — *Output current vs. error voltage V_{EAO}*

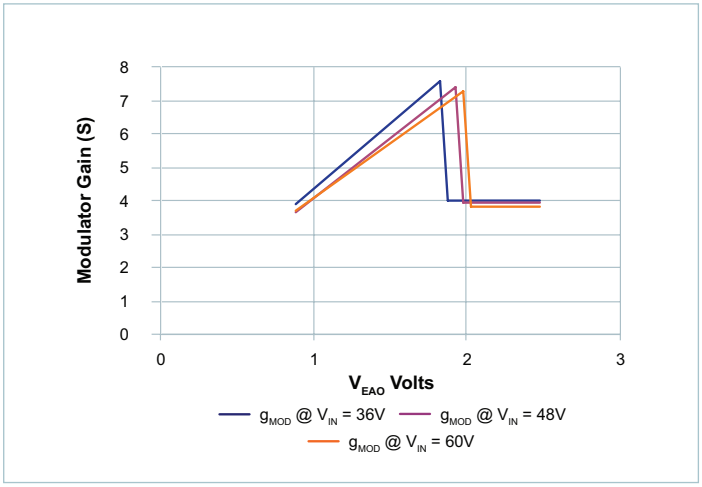


Figure 35 — *Modulator gain vs. error voltage V_{EAO}*

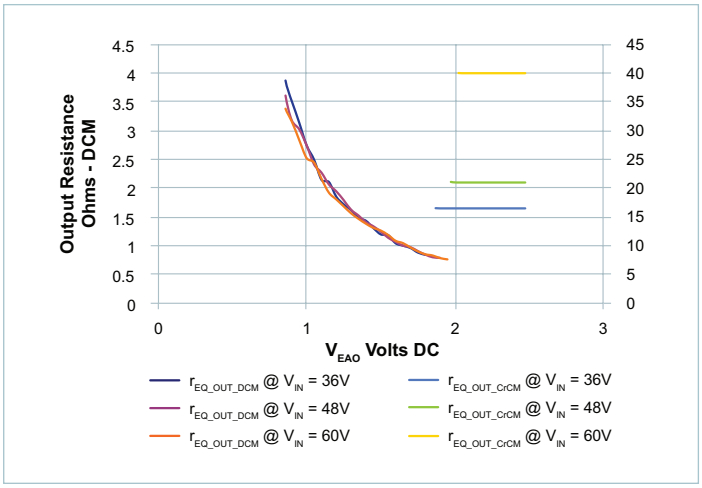


Figure 36 — *Output equivalent resistance vs. error voltage V_{EAO}*

PI3546-00 (12.0V_{OUT}) Electrical Characteristics

Specifications apply for –40°C < T_J < 125°C, V_{IN} = 48V, EN = High, V_{VDR} = 5.1V ±2%, L1 = 900nH [a] unless other conditions are noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Specifications						
Input Voltage	V_{IN_DC}		36	48	60	V
Input Voltage, Transient	V_{IN_TRANS}	< 1% duty cycle,entire transient duration < 10ms			70	V
Input Current	I_{IN_DC}	V_{IN} = 48V, T_C = 25°C, I_{OUT} = 9A		2.33		A
Input Current At Output Short (Fault Condition Duty Cycle)	I_{IN_Short}	Short at terminals		3.3	-	mA
Input Quiescent Current	I_{Q_VIN}	Disabled		0.75		mA
		Enabled (no load)		2.6		
Input Voltage Slew Rate	V_{IN_SR}				1	V/µs
Output Specifications						
EAIN Voltage Total Regulation	V_{EAIN}	[b]	0.985	1.00	1.015	V
Output Voltage Trim Range	V_{OUT_DC}	[b] [c]	6.5	12	14	V
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	@ 25°C, 36V < V_{IN} < 60V		0.10		%
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	@ 25°C, 0.5A < I_{OUT} < 9A		0.10		%
Output Voltage Ripple	V_{OUT_AC}	I_{OUT} = 9A, C_{OUT} = 6 x 10µF, 20MHz BW [d]		114		mVp-p
Output Current	I_{OUT_DC}	[e]	0		9	A
Maximum Array Size	$N_{Parallel}$				3	Modules
Output Current, Array of 2	$I_{OUT\_DC\text{-}ARRAY2}$	Total array capability, see applications section for details	0		15.9	A
Output Current, Array of 3	$I_{OUT\_DC\text{-}ARRAY2}$	Total array capability, see applications section for details	0		22.9	A
Current Limit	I_{OUT_CL}	Typ limit based on nominal 900nH inductor.		10.5		A
Timing						
Switching Frequency	f_S	[f] 48V_{IN} to 12V_{OUT}, 2A out, L1 = 900nH ±1%	-	800	-	kHz
Fault Restart Delay	t_{FR_DLY}			30		ms

[a] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI354x evaluation board with 2.5 x 4in dimensions and 4-layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[b] Regulator is assured to meet performance specifications by design, test correlation, characterization and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[c] Output current capability may be limited and other performance may vary from noted electrical characteristics when V_{OUT} is not set to nominal.
[d] Refer to output ripple plots.
[e] Refer to load current vs. ambient temperature curves.
[f] Refer to switching frequency vs. load current curves.

PI3546-00 (12.0V_{OUT}) Electrical Characteristics (Cont.)

Specifications apply for –40°C < T_J < 125°C, V_{IN} = 48V, EN = High, V_{VDR} = 5.1V ±2%, L1 = 900nH [a] unless other conditions are noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Soft Start, Tracking and Error Amplifier						
TRK Active Range (Nominal)	V_{TRK}		0		1.4	V
TRK Enable Threshold	V_{TRK_OV}		20	40	60	mV
TRK to EAIN Offset	V_{EIAN_OV}	V_{TRK} = 0.5V, EA0 shorted to EAIN	50	80	110	mV
Charge Current (Soft-Start)	I_{TRK}		70	50	30	µA
Discharge Current (Fault)	I_{TRK_DIS}	V_{TRK} = 0.5V		10		mA
Soft-Start Time	t_{SS}	C_{TRK} = 0µF	0.6	0.94	1.6	ms
Error Amplifier Trans-Conductance	GM_{EAO}	[b]		7.6		mS
PSM Skip Threshold	PSM_{SKIP}	[b]		0.8		V
Error Amplifier Output Impedance	R_{OUT}	[b]	1			MΩ
Internal Compensation Capacitor	C_{HF}	[b]		56		pf
Internal Compensation Resistor	R_{ZI}	[b]		5		kΩ

[a] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI354x evaluation board with 2.5 x 4in dimensions and 4-layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[b] Regulator is assured to meet performance specifications by design, test correlation, characterization and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[c] Output current capability may be limited and other performance may vary from noted electrical characteristics when V_{OUT} is not set to nominal.
[d] Refer to output ripple plots.
[e] Refer to Load current vs. ambient temperature curves.
[f] Refer to switching frequency vs. load current curves.

PI3546-00 (12.0V_{OUT}) Electrical Characteristics (Cont.)

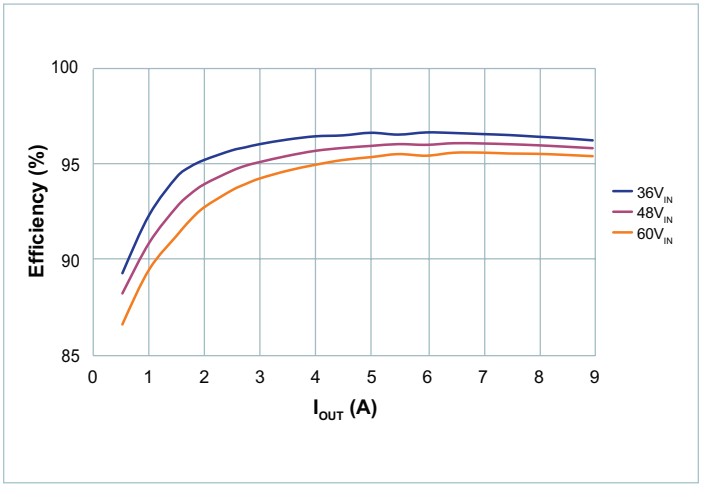


Figure 37 — *Regulator efficiency*

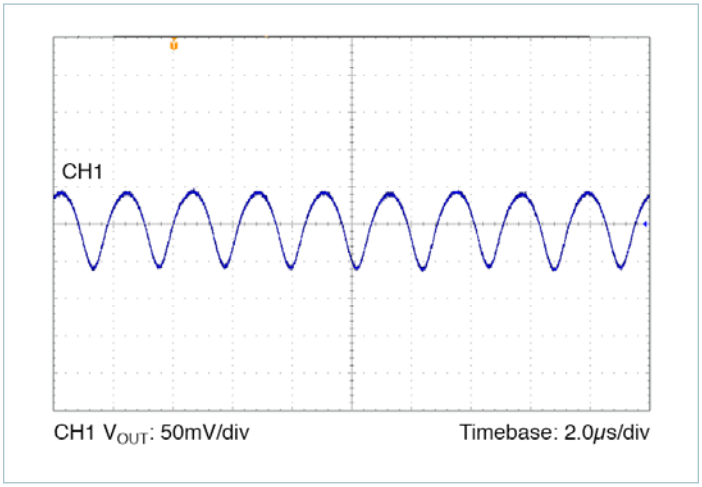


Figure 40 — *Output ripple: 48V_{IN}, 12.0V_{OUT} at 9A.*
V_{OUT} = 50mV/Div, 2.0µs/Div;
C_{OUT} = 6 x 10µF ceramic

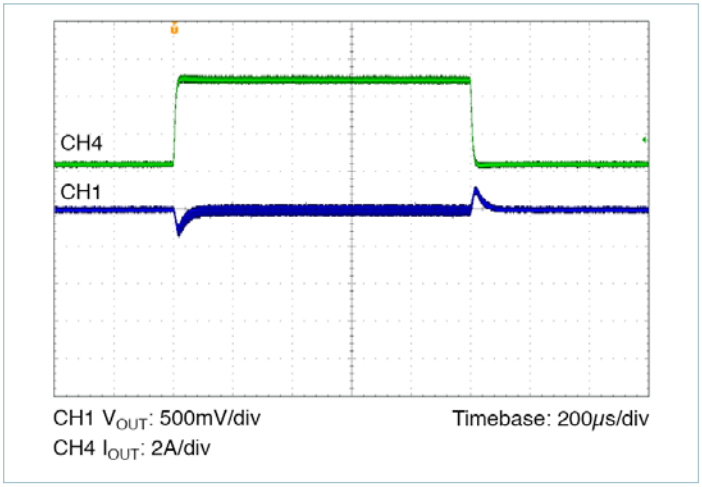


Figure 38 — *Transient response: 5A to 10A, at 1A/µs. 48V_{IN} to 12.0V_{OUT}, C_{OUT} = 6 x 10µF ceramic*

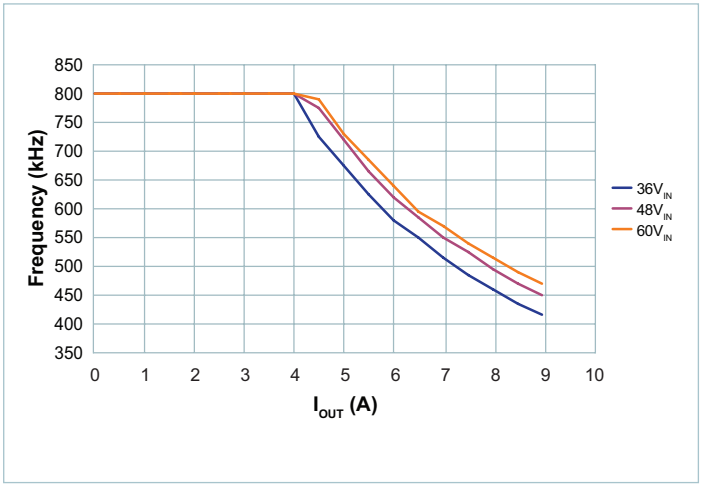


Figure 41 — *Switching frequency vs. load current*

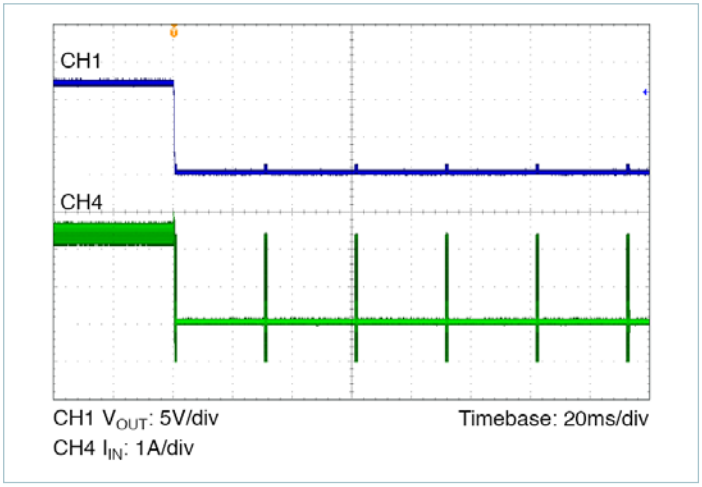


Figure 39 — *Output short circuit @ V_{IN} = 48V*

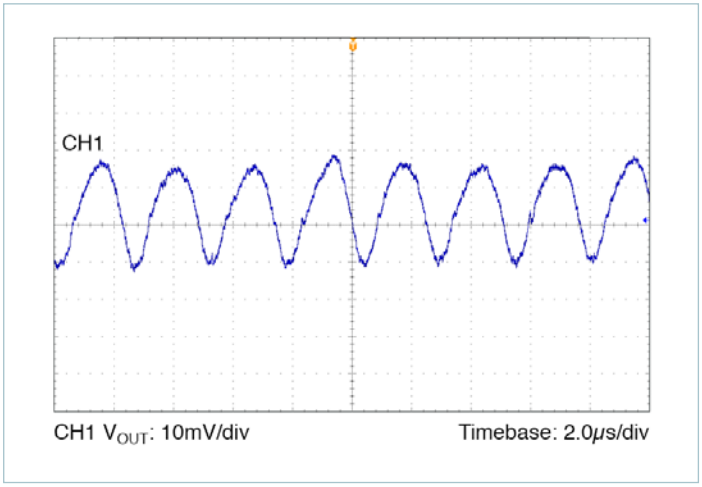


Figure 42 — *Output ripple: 48V_{IN}, 12.0V_{OUT} at 4.5A.*
V_{OUT} = 10mV/Div, 2.0µs/Div;
C_{OUT} = 6 x 10µF ceramic

PI3546-00 (12.0V_{OUT}) Electrical Characteristics (Cont.)

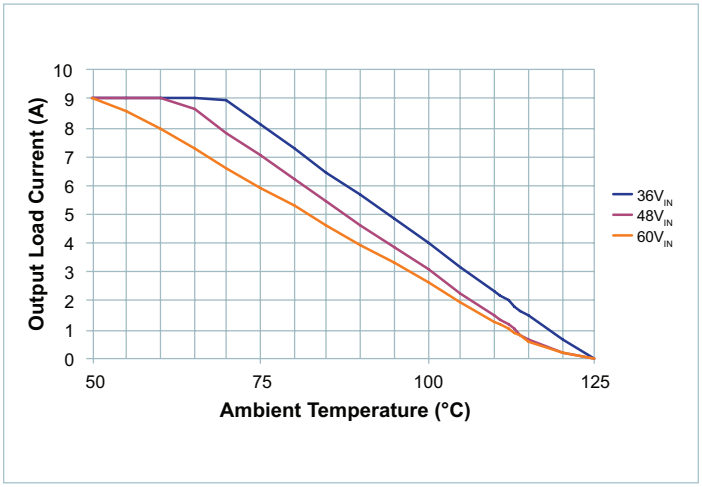


Figure 43 — *Load current vs. ambient temperature, 0LFM*

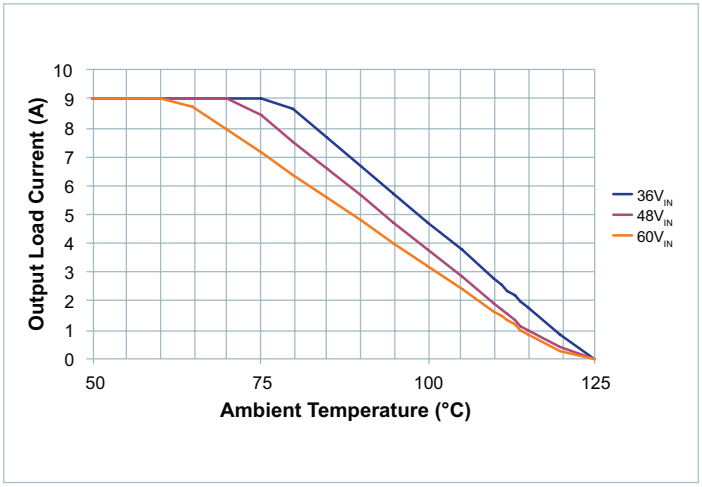


Figure 44 — *Load current vs. ambient temperature, 200LFM*

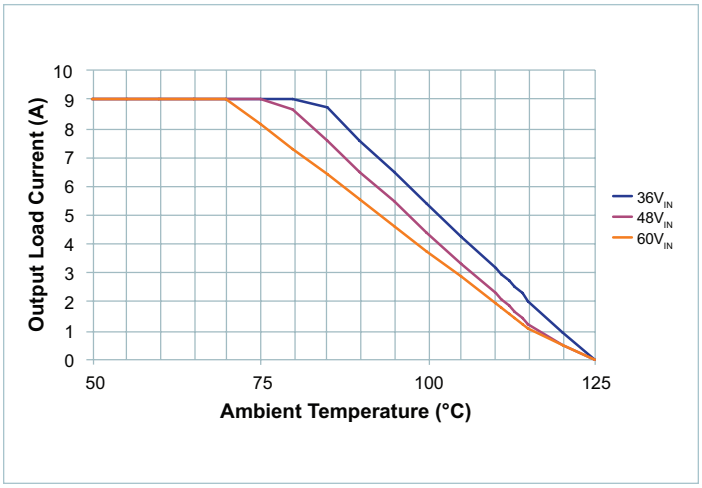


Figure 45 — *Load current vs. ambient temperature, 400LFM*

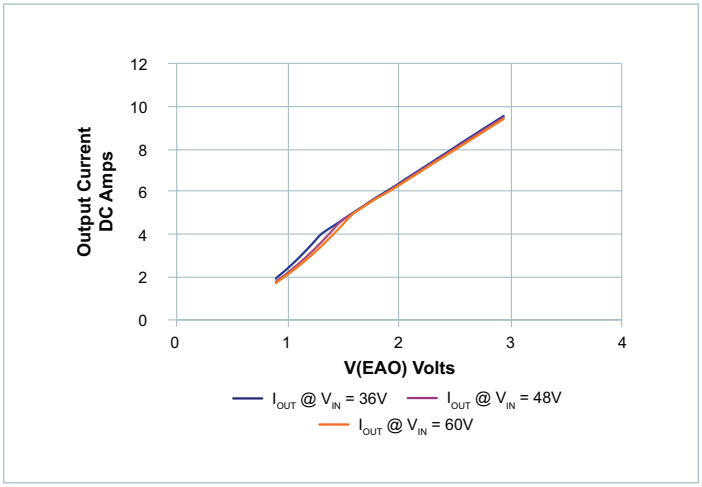


Figure 46 — *Output current vs. error voltage V_{EAO}*

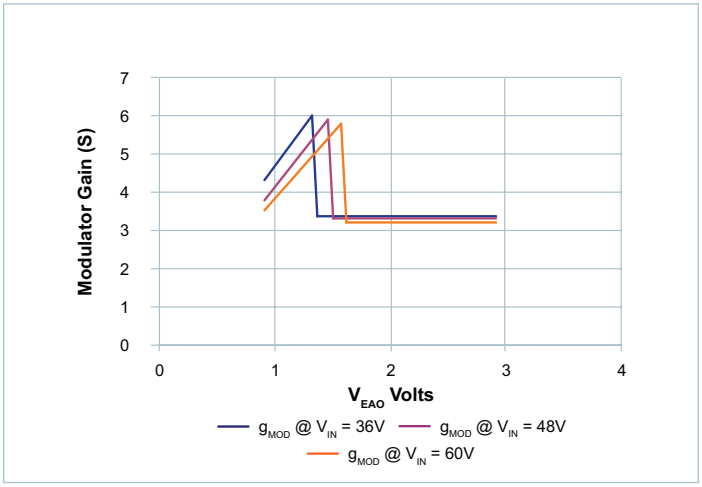


Figure 47 — *Modulator gain vs. error voltage V_{EAO}*

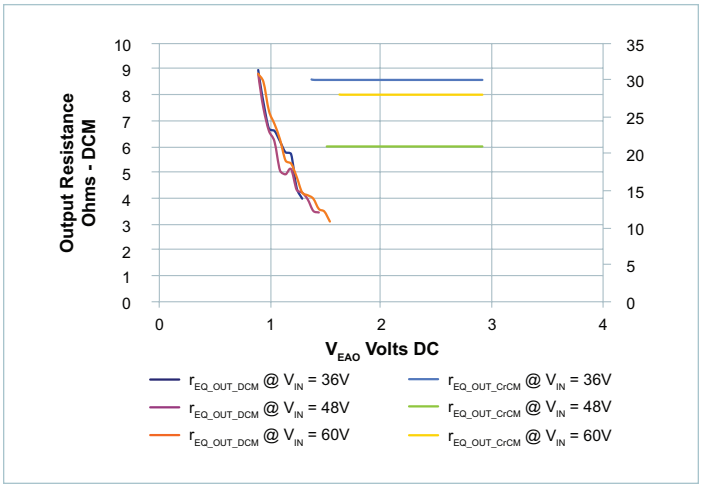


Figure 48 — *Output equivalent resistance vs. error voltage V_{EAO}*

Functional Description

The PI354x-00 is a family of highly integrated ZVS Buck regulators. The PI354x-00 has an output voltage that can be set within a prescribed range shown in Table 1. Performance and maximum output current are characterized with a specific external power inductor (see Table 2).

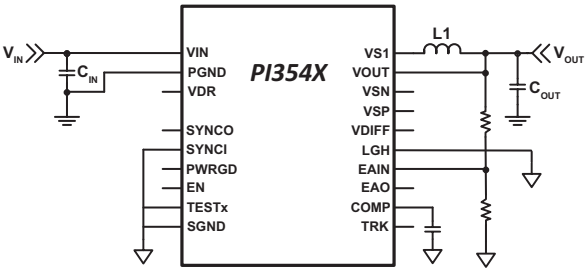


Figure 49 — *ZVS Buck with required components*

For basic operation, Figure 49 shows the connections and components required. No additional design or settings are required.

ENABLE (EN)

EN is the enable pin of the converter. The EN Pin is referenced to SGND and permits the user to turn the regulator on or off. The EN default polarity is a positive logic assertion. If the EN pin is left floating or asserted high, the converter output is enabled. Pulling EN pin below $0.8V_{DC}$ with respect to SGND will disable the regulator output.

Remote Sensing

If remote sensing is required, the PI354x-00 product family is equipped with an undedicated differential amplifier. This amplifier can allow full differential remote sense by configuring it as a differential follower and connecting the VDIFF pin to the EAIN pin.

Switching Frequency Synchronization

The SYNCO pin provides a 5V level clock that can be used to monitor the internal clock of the regulator, or synchronize other regulators to it. The start of the switching cycles will coincide with the rising edge of SYNCO, and SYNCO will remain high for ½ the period of the preset switching frequency (f_S), or T1, whichever is longer. The SYNCI input allows the controller to synchronize its internal clock to an external clock source. The SYNCI pin should be connected to SGND through a 0Ω resistor when not in use and should never be left floating. The controller can synchronize to frequencies between 50% and 110% of the preset switching frequency (f_S). When using SYNCI, the PI354x-00 phase synchronizes to the falling edge of the applied clock on SYNCI. When SYNCI is driven from a second module's SYNCO, there is an effective 180 degrees of phase shift between the start of the switching cycles, provided the modules are switching at the preset switching frequency. At higher loads when pulse stretching occurs and the operating frequency is lowered, the phase shift is no longer 180 degrees. Also when the switching frequency of a module is reduced due to an external clock source driving SYNCI, the current limit threshold may be significantly reduced.

Soft-Start

The PI354x-00 includes an internal soft-start capacitor to control the rate of rise of the output voltage. See the Electrical Characteristics Section for the default value. Connecting an external capacitor from the TRK pin to SGND will increase the start-up ramp period. See, "Soft Start Adjustment and Track," in the Applications Description section for more details.

Output Voltage Selection

The PI354x-00 output voltage can be selected by connecting a resistor from EAIN pin to SGND and a resistor from Vout to the EAIN pin as shown in Figure 49. Table 1 defines the allowable operational voltage ranges for the PI354x-00 family.

Device	Output Voltage	
	Nom.	Range
PI3542-00-xGIZ	2.5V	2.2 – 3.0V
PI3543-00-xGIZ	3.3V	2.6 – 3.6V
PI3545-00-xGIZ	5.0V	4.0 – 5.5V
PI3546-00-xGIZ	12V	6.5 – 14.0V

Table 1 — *PI354x-00 family output voltage ranges*

Output Current Limit Protection

PI354x-00 has two methods implemented to protect from output short or over current condition.

Slow Current Limit protection: prevents the output from sourcing current higher than the regulator's maximum rated current. If the output current exceeds the Current Limit (I_{OUT_CL}) for 1024µs, a slow current limit fault is initiated and the regulator is shut down, which eliminates output current flow. After Fault Restart Delay (t_{FR_DLY}), a soft-start cycle is initiated. This restart cycle will be repeated indefinitely until the excessive load is removed.

Fast Current Limit protection: PI354x-00 monitors the regulator inductor current pulse-by-pulse to prevent the output from supplying very high current due to sudden low-impedance short. If the regulator senses a high inductor current pulse, it will initiate a fault and stop switching until Fault Restart Delay ends and then initiate a soft-start cycle.

Input Undervoltage Lockout

If V_{IN} falls below the input Undervoltage Lockout (UVLO) threshold, but remains high enough to power the internal bias supply, the PI354x-00 will complete the current cycle and stop switching. The system will soft start once the input voltage is reestablished and after the Fault Restart Delay.

Input Overvoltage Lockout

If V_{IN} exceeds the input Overvoltage Lockout (OVLO) threshold (V_{OVLO}), while the controller is running, the PI354x-00 will complete the current cycle and stop switching. The system will soft start after the Fault Restart Delay once V_{IN} recovers. The PI354x products permit input voltage positive transient excursions beyond V_{IN_DC} maximum, up to $V_{IN\text{-}TRANS}$ maximum. In this case, the input voltage is allowed to be outside the V_{IN_DC} range for up to 10ms, with no more than a 1% duty cycle. Note that any excursion beyond the V_{IN_DC} maximum must still adhere to the maximum slew rate V_{IN_SR}.

Output Overvoltage Protection

The PI354x-00 family is equipped with output Overvoltage Protection (OVP) to prevent damage to input voltage sensitive devices. If the output voltage exceeds 20% of its set regulated value, the regulator will complete the current cycle and stop switching. The system will resume operation once the output voltage falls below the OVP threshold and after Fault Restart Delay.

Overtemperature Protection

The PI354x features an over temperature protection (OTP), which will not engage until after the product is operated above the maximum rated temperature. The OTP circuit is only designed to protect against catastrophic failure due to excessive temperatures and should not be relied upon to ensure the device stays within the recommended operating temperature range. Thermal shut down terminates switching and discharges the soft-start capacitor. As the temperature falls the PI354x will restart, and this will always occur before the product returns to rated temperature range.

Pulse Skip Mode (PSM)

PI354x-00 features a PSM to achieve high efficiency at light loads. The regulators are setup to skip pulses if EAO falls below a PSM threshold. Depending on conditions and component values, this may result in single pulses or several consecutive pulses followed by skipped pulses. Skipping cycles significantly reduces gate drive power and improves light load efficiency. The regulator will leave PSM once the EAO rises above the Skip Mode threshold.

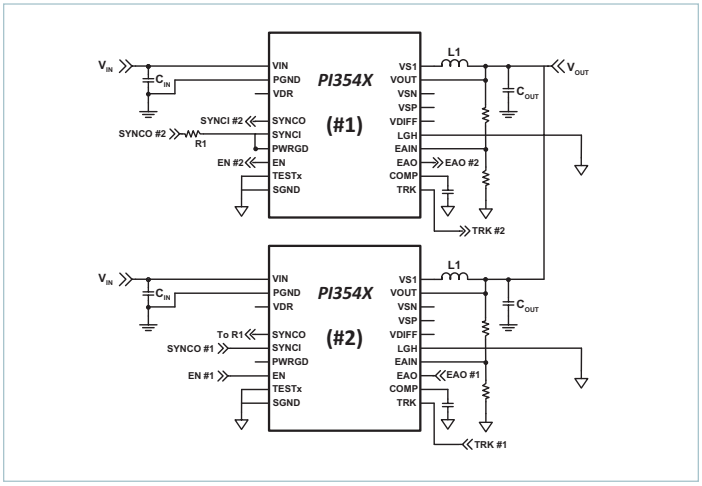


Figure 50 — *PI354x-00 parallel operations*

Variable Frequency Operation

Each PI354x-00 is preprogrammed to a base operating frequency, with respect to the power stage inductor (see Table 2), to operate at peak efficiency across line and load variations. At low-line and high-load applications, the base frequency will decrease to accommodate these extreme operating ranges. By stretching the frequency, the ZVS operation is preserved throughout the total input line voltage range therefore maintaining optimum efficiency.

Application Description

Parallel Operation

PI354x-00 can be connected in parallel to increase the output capability of a single output rail. When connecting modules in parallel, each EAO, TRK, EAIN and EN pin should be connected together. Current sharing will occur automatically in this manner so long as each inductor is the same value. A common viewing chain may be used to sense the output voltage. Refer to the Electrical Characteristics table for maximum array size and array rated output current. Current sharing may be considered independent of synchronization and/or interleaving. Modules do not have to be interleaved or synchronized to share current.

Synchronization

PI354x-00 units may be synchronized to an external clock by driving the SYNCI pin. The synchronization frequency must not be higher than the programmed maximum value F_{SW}. This is the switching frequency during DCM of operation. The minimum synchronization frequency is F_{SW} /2. In order to ensure proper power delivery during synchronization, the user should refer to the switching frequency vs. output current curves for the load current, output voltage and input voltage operating point. The synchronization frequency should not be lower than that determined by the curve or reduced output power will result. The power reduction is approximately the ratio between required frequency and synchronizing frequency. If the required frequency is 1MHz and the sync frequency is 600kHz, the user should expect a 40% reduction in output capability.

Interleaving

Interleaving is primarily done to reduce output ripple and the required number of output capacitors by introducing phase current cancellation. The PI354x-00 has a fixed delay that is proportional to to the maximum value of F_{SW} shown in the data sheet. When connecting two units as shown in Figure 50, they will operate at 180 degrees out of phase when the converters switching frequency is equal to F_{SW}. If the converter enters CrCM and the switching frequency is lower than F_{SW}, the phase delay will no longer be 180 degrees and ripple cancellation will begin to decay. Interleaving when the switching frequency is reduced to lower than 80% of the programmed maximum value is not recommended.

Output Voltage Set Point

The PI354x-00 family of Buck Regulators utilizes an internal reference (V_{REF}). The output voltage setting is accomplished using external resistors as shown in Figure 51. Select R2 to be at or around 1kΩ for best noise immunity. Use Equations 1 and 2 to determine the proper value based on the desired output voltage.

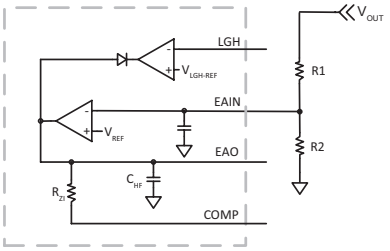


Figure 51 — *External resistor divider network*

$$V_{OUT} = V_{REF} \bullet \frac{R1 + R2}{R2} \qquad (1)$$

$$R1 = R2 \bullet \frac{(V_{OUT} - V_{REF})}{V_{REF}} \qquad (2)$$

$$where \quad V_{REF} = V_{EAIN}$$

Soft-Start Adjust and Tracking

The TRK pin offers a means to increase the regulator's soft-start time or to track with additional regulators. The soft-start slope is controlled by an internal capacitor and a fixed charge current to provide a Soft-Start Time t_{SS} for all PI354x-00 regulators. By adding an additional external capacitor to the TRK pin, the soft-start time can be increased further. The following Equation can be used to calculate the proper capacitor for a desired soft-start times:

$$C_{TRK} = (t_{TRK} \bullet I_{TRK}) - 47 \bullet 10^{-9} \qquad (3)$$

Where, t_{TRK} is the soft-start time and I_{TRK} is a 50µA internal charge current (see Electrical Characteristics for limits).

There is typically either proportional or direct tracking implemented within a design. For proportional tracking between several regulators at start up, simply connect all PI354x-00 device TRK pins together. This type of tracking will force all connected regulators to start up and reach regulation at the same time (see Figure 52a).

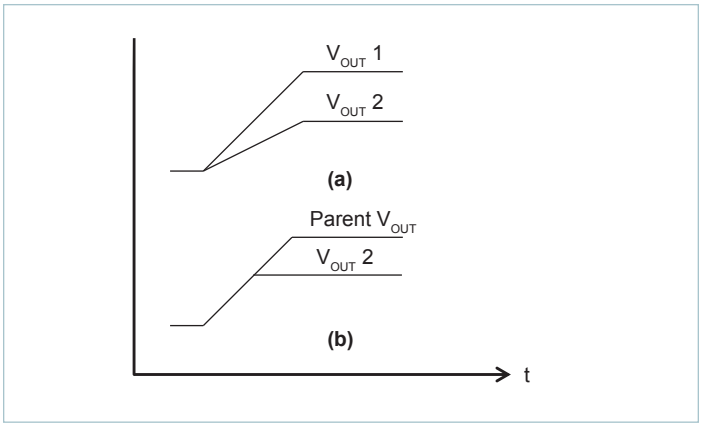


Figure 52 — *PI354x-00 tracking methods*

For Direct Tracking, choose the PI354x-00 with the highest output voltage as the parent and connect the parent to the TRK pin of the other PI354x-00 regulators through a divider (Figure 53) with the same ratio as the child's feedback divider.

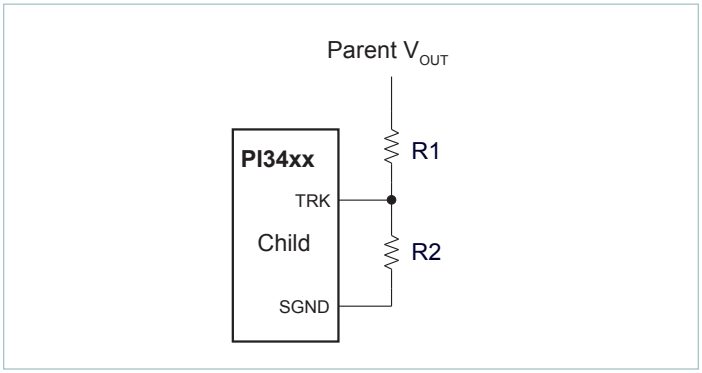


Figure 53 — *Voltage divider connections for direct tracking*

All connected PI354x-00 regulator soft-start slopes will track with this method. Direct tracking timing is demonstrated in Figure 52b. All tracking regulators should have their Enable (EN) pins connected together to work properly.

Inductor Pairing

The PI354x-00 utilizes an external inductor. This inductor has been optimized for maximum efficiency performance. Table 2 details the specific inductor value and part number utilized for each PI354x-00.

Device	Inductor (nH)	Inductor Part Number	Manufacturer
PI3542-00	340	FPT1006-340-R	Eaton
PI3543-00	420	HCV1206-R42-R	Eaton
		PA5119.421NLT	Pulse
PI3545-00	420	HCV1206-R42-R	Eaton
		PA5119.421NLT	Pulse
PI3546-00	900	HCV1206-R90-R	Eaton
		PA5119.901NLT	Pulse

Table 2 — *PI354x-00 inductor pairing*

Thermal De-Rating

Thermal de-rating curves are provided that are based on component temperature changes versus load current, input voltage and air flow. It is recommended to use these curves as a guideline for proper thermal de-rating. These curves represent the entire system and are inclusive to both the Picor regulator and the external inductor. Maximum thermal operation is limited by either the MOSFETs or inductor depending upon line and load conditions.

Thermal measurements were made using a standard PI354x-00 Evaluation board which is 2.5 x 4 inches in area and uses 4-layer, 2oz copper. Thermal measurements were made on the three main power devices, the two internal MOSFETs and the external inductor, with air flows of 0, 200, and 400LFM.

Small Signal Model – Constant Voltage Mode

The PI354x-00 product family is a variable frequency CCM/DCM ZVS Buck Regulator. The small signal model for this powertrain is that of a voltage controlled current source which has a trans-conductance that varies depending on the operating mode. When the converter is operating at its normal frequency, it is in discontinuous mode. As the load increases to the point at which the boundary between discontinuous and continuous modes is reached, the powertrain changes frequency to remain in critical conduction mode. This mode of operation allows the PI354x-00 product family to have a very simple compensation scheme, as the control to output transfer function always has a slope of –1. In addition, when critical conduction is reached, the voltage controlled current source becomes nearly ideal with a high output equivalent resistance.

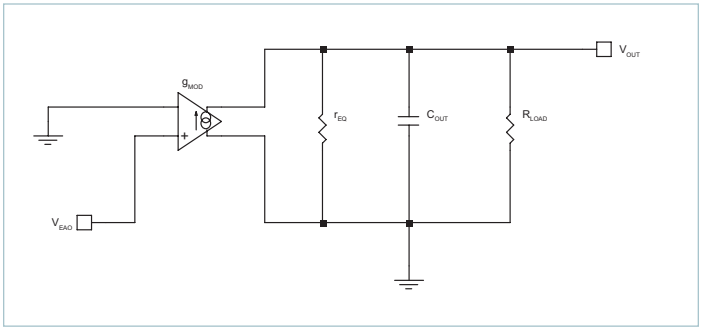


Figure 54 — *PI354x-00 small-signal model control-output*

The control to output transfer function of the PI354x-00 product family is defined as the gain from the output of the error amplifier, through the modulator and to the output voltage. The transfer function Equation is shown in Equation 4, where g_{MOD} is assumed to be 7S, r_{EQ} = 0.4Ω, C_{OUT} = 600µF and R_{LOAD} = 1Ω:

$$G_{CO}(s) = \frac{g_{MOD}}{\frac{1}{R_{LOAD}} + \frac{1}{r_{EQ}} + s\left(C_{OUT}\right)} \qquad (4)$$

The Control-Output transfer function (also known as the small signal modulator gain) has a single pole response determined by the parallel combination of R_{LOAD} and r_{EQ} and the output capacitor C_{OUT}. Equation 5 determines the frequency of the modulator pole:

$$F_{P\_MOD} = \frac{1}{2 \bullet \pi \bullet \frac{R_{LOAD} \bullet r_{EQ}}{R_{LOAD} + r_{EQ}} \bullet C_{OUT}} \qquad (5)$$

Figure 55 depicts the small signal response of the modulator when perturbing EAO and measuring the differential gain and phase from EAO to V_{OUT}.

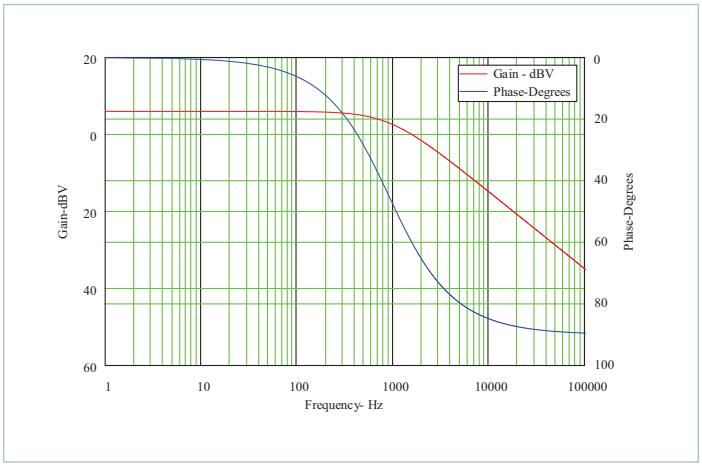


Figure 55 — *PI354x-00 control-output gain/phase example*

Error Amplifier

The small signal model of the error amplifier and compensator is shown in Figure 56. The error amplifier is a transconductance amplifier (TCA). The transfer function is shown in Equation 6, where in this example R1 = 2.3kΩ, R2 = 1kΩ, GM_{EAO} = 5.1mS, R_{OUT} = 1Meg, C_{HF} = 56pF, Ccomp = 4.7nF and R_{ZI} = 5kΩ. Here it is important to note that the external components are Ccomp, R1 and R2. The other components are internal to each specific model. See the data tables section "Soft Start, Tracking And Error Amplifier" for details.

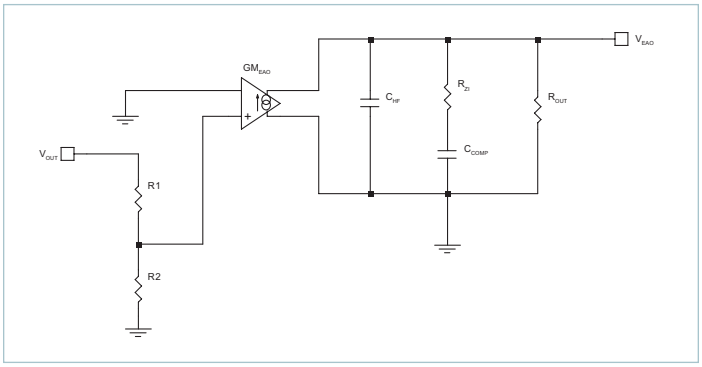


Figure 56 — *PI354x-00 error amplifier model*

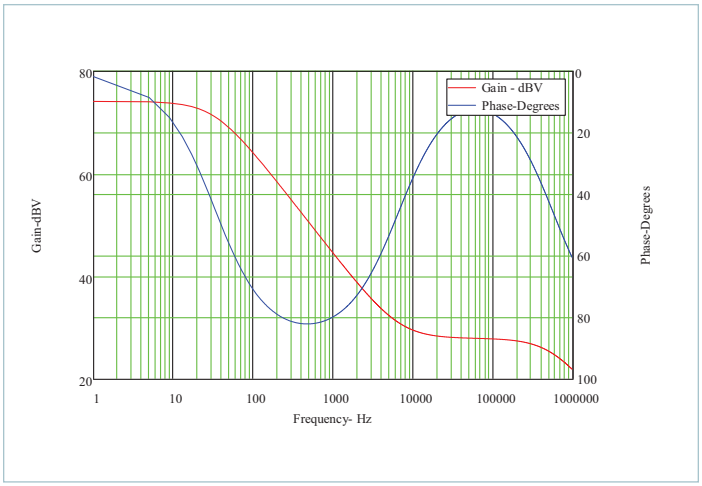


Figure 57 — *PI354x-00 input-control gain/phase*

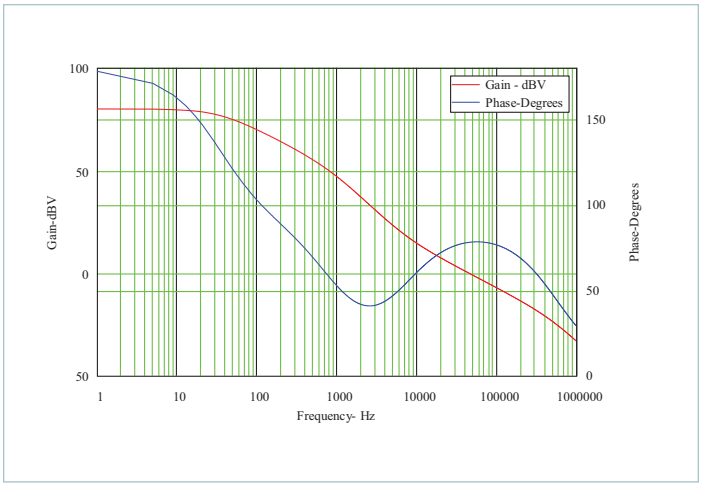


Figure 58 — *PI354x-00 output-input gain/phase*

$$G_{IN\_CTL}(s) = GM_{EAO} \bullet \frac{R_{OUT} + s\left(R_{ZI} \bullet C_{COMP} \bullet R_{OUT}\right)}{1 + s \bullet \left(C_{COMP} \bullet (R_{OUT} + R_{ZI}) + R_{OUT} \bullet C_{HF}\right) + s^2 \bullet \left(C_{HF} \bullet C_{COMP} \bullet R_{ZI} \bullet R_{OUT}\right)} \bullet \frac{R2}{R1 + R2} \quad (6)$$

The transfer function of the error amplifier and compensator (also known as the Input To Control transfer function) reveals the response of a Type II amplifier with a low-frequency pole determined by Equation 7, a zero which sets the mid-band gain determined by Equation 8 and a high-frequency pole determined by Equation 9. Figure 58 shows the calculated Input To Control transfer function. Multiplying Equation 3 by Equation 6 ; described by Equation 10, results in the total loop gain (also known as the Output To Input transfer function). A graph is shown in Figure 58. The strategy is to set the zero such that the mid-band gain allows a high crossover frequency while providing maximum phase boost at crossover, with proper gain and phase margin.

$$F_{PLF} = \frac{1}{2 \bullet \pi \bullet \left(R_{ZI} + R_{OUT}\right) \bullet \left(C_{COMP} + C_{HF}\right)} = 33Hz \quad (7)$$

$$F_{ZMB} = \frac{1}{2 \bullet \pi \bullet \left(R_{ZI} // R_{OUT}\right) \bullet C_{COMP}} = 6.8kHz \quad (8)$$

$$F_{PHF} = \frac{C_{HF} + C_{COMP}}{2 \bullet \pi \bullet (R_{ZI} // R_{OUT}) \bullet C_{COMP} \bullet C_{HF}} = 580kHz \quad (9)$$

$$G_{OUT\_IN}(s) = G_{CO}(s) \bullet G_{IN\_CTL}(s) \quad (10)$$

Lighting Mode (LGH)

The Lighting (LGH) mode allows the PI354x-00 product family to be able to operate in constant current mode (CC) so that it can support a wide range of applications that require the ability to regulate current or voltage. Primary applications are LED lighting, battery / super-capacitor charging and high peak current pulse transient load applications. The PI354x-00 product family can operate in dual modes, either as a constant voltage (CV) regulator or a constant current (CC) regulator. Both modes can be utilized in a single system. The PI354x-00 family has a separate current amplifier, called LGH, and built in 100mV lighting reference that has its output connected to the EAO pin internally. If the current through an external shunt starts to develop 100mV at the LGH pin, the LGH amplifier will take over regulation by pulling down on the EAO output until the current is in regulation according to the designed shunt value. The LGH amplifier is a sink only trans-conductance amplifier (TCA). It does not source current. In the event of an open LED string or open current signal, the voltage loop can be set to regulate the output voltage to a safe or desired value in CV mode.

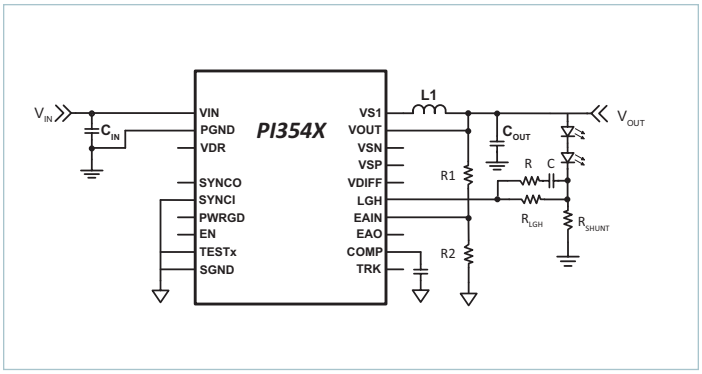


Figure 59 — *Lighting configuration using CC mode*

When using the CC mode, it is important to set R1 and R2 appropriately to avoid voltage loop interaction with the current loop. In this case, the voltage setting at the EAIN pin should be set so that the error between it and the 1V reference is sufficient to force the EAO to be open loop and source current always. When not using the LGH amplifier, the LGH pin should be connected to SGND.

The LGH amplifier is able to sink more current than the error amplifier can source, thus avoiding arbitration issues when transitioning back and forth from LGH mode to voltage mode. The Equation for setting the source current for EAO is shown in Equation 11.

$$I_{EAO} = (V_{EAIN} - V_{REF}) \bullet G_{MEA} > 400\mu A \qquad (11)$$

LGH Amplifier Small Signal Model

A small signal model of the LGH amplifier is shown in Figure 60.

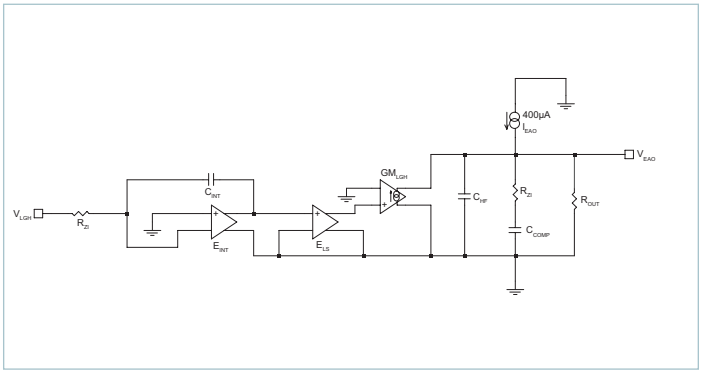


Figure 60 — *LGH amplifier small-signal model*

The LGH amplifier consists of three distinct stages. The first is a wide bandwidth integrator stage, followed by a fixed gain level shift circuit. Finally, the level shift circuit drives a trans-conductance (TCA) amplifier with an open collector sink only output stage. Since the LGH output is internally connected to the output of the voltage error amplifier, the compensation components show up in the model and are used by both stages, depending on which one is in use. Only one stage should be in use at a time. When using LGH or if the LGH input rises above the internal reference, the voltage error amplifier acts as a 400µA current source pull up for the EAO pin.

Figure 61 shows a small signal model of the modulator gain when using the application circuit shown in Figure 59 with two 3.4V high-current LED's in series. R_{LED} is the series combination of the AC resistance of each LED, which is 0.2Ω. R_{SHUNT} is used to sense the current through the LED string. It has a value of 50mΩ in this case. The other component values were defined earlier and remain the same values. Equation 12 defines the transfer function of the modulator and Equation 13 defines the pole of transfer function. The transfer function of the LGH amplifier is defined in Equation 14. The open loop gain of E_{INT} is 2500 and E_{LS} = 4.4.

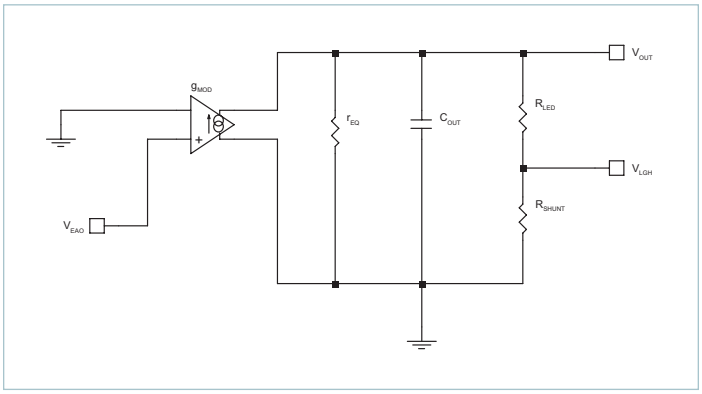


Figure 61 — *Lighting application modulator gain model*

Figure 62 is the Bode plot of the $G_{LED}(s)$ transfer function, which in LGH mode is what needs to be compensated for by the LGH amplifier and compensator. This transfer function defines the gain and phase from the error amplifier output (EAO) to the current shunt R_{SHUNT}. Figure 65 is a plot of the transfer function $G_{LGH\_EAO}(s)$, which defines the gain and phase from the LGH pin (voltage across current sensing R_{SHUNT}) to EAO. As shown in Equation 14, the output is dependent on the integrator stage and the following transconductance stage. Figures 63 and 64 show the two individual sections that make up Equation 14 which produces $G_{LGH\_EAO}(s)$.

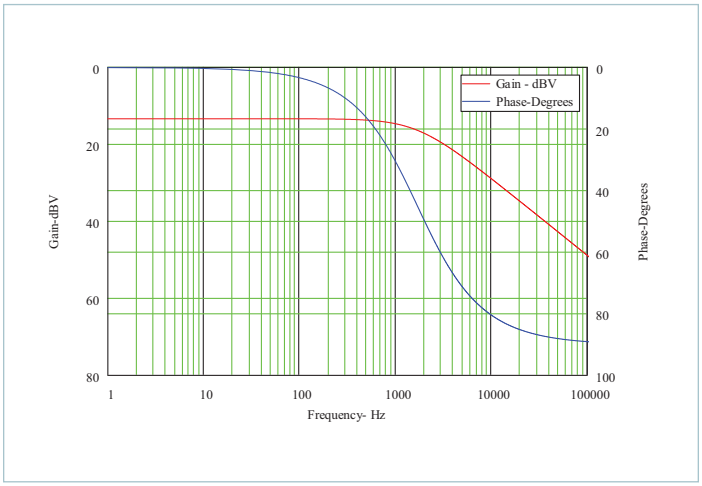


Figure 62 — *$G_{LED}(s)$ gain/phase plot*

$$G_{LED}(s) = g_{MOD} \bullet \left(r_{EQ} \bullet R_{SHUNT}\right) / \left(\left(R_{SHUNT} + R_{LED} + r_{EQ}\right) + s\left(C_{OUT} \bullet r_{EQ} \bullet R_{LED} + R_{SHUNT} \bullet r_{EQ} \bullet C_{OUT}\right)\right) \quad (12)$$

$$F_{P\_LED} = \frac{1}{2 \bullet \pi \bullet \left(\left(R_{LED} + R_{SHUNT}\right) // r_{EQ}\right) \bullet C_{OUT}} = 1.2kHz \quad (13)$$

$$G_{LGH\_EAO}(s) = E_{INT}(s) \bullet E_{LS} \bullet GM_{LGH} \bullet \frac{R_{OUT} + s\left(R_{ZI} \bullet C_{COMP} \bullet R_{OUT}\right)}{1 + s \bullet \left(C_{COMP} + C_{HF}\right) + s^2 \bullet \left(C_{HF} \bullet C_{COMP} \bullet R_{ZI}\right)} \quad (14)$$

Where:

$$E_{INT}(s) = E_{INT} \bullet \frac{1}{1 + s \bullet \left(R_{LGH} \bullet C_{INT} \bullet E_{INT}\right)} \quad (15)$$

$$F_{P\_HF} = \frac{C_{HF} + C_{COMP}}{2 \bullet \pi \bullet \left(R_{ZI} // R_{OUT}\right) \bullet C_{COMP} \bullet C_{HF}} = 580kHz \quad (16)$$

The integrator pole is determined by the external input resistor R_{LGH} and the internal C_{INT}, which is 20pF. Assuming R_{LGH} = 100kΩ and E_{INT} = 2500:

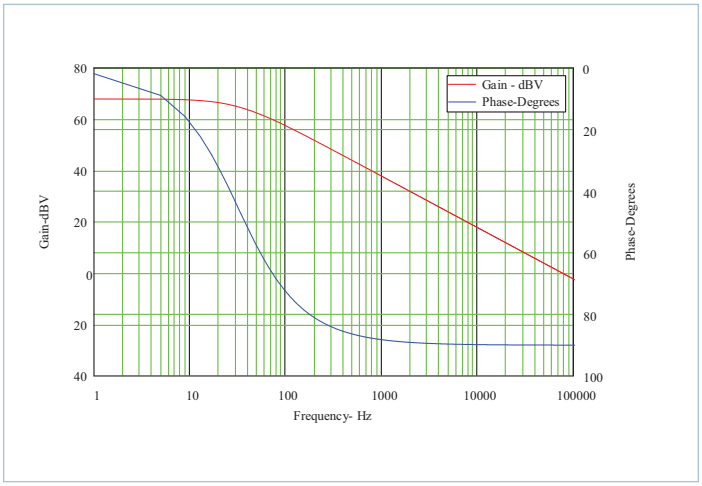


Figure 63 — *E_{INT}(s) gain/phase plot R_{LGH} = 100kΩ*

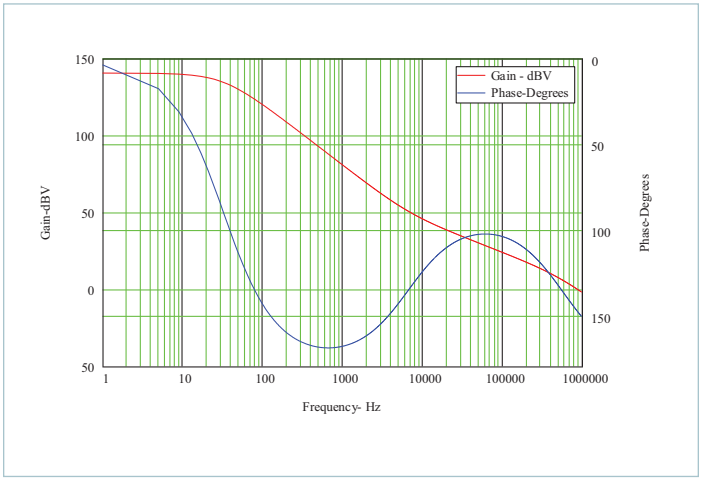


Figure 65 — *G_{LGH_EAO}(s) gain/phase plot R_{LGH} = 100kΩ*

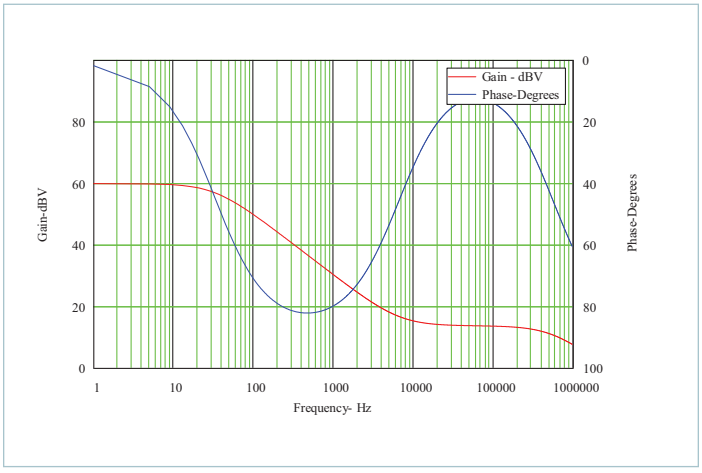


Figure 64 — *GM_{LGH}(s) gain/phase plot voltage loop open*

When combining Figure 63 with Figure 64, it becomes clear that additional compensation is needed to have enough phase and gain margin like can be seen with the voltage loop plot. We can remedy that easily, by adding a series R-C in parallel with R_{LGH} as shown in the lighting application diagram in Figure 59. The capacitor will be chosen to work with R_{LGH} to add a zero approximately 1.2kHz before the zero provided by the GM_{LGH}(s) transfer function (the trans-conductance stage of the LGH amplifier). This value will be chosen to be 270pF. The external added resistor will form a high-frequency pole to roll the gain off at higher frequency. This pole will be set at approximately 120kHz so a common 4.99kΩ resistor will be used. The resulting Bode plot with the new compensator of G_{LGH_EAO}(s) can be seen in Figure 66. Figure 67 shows the final Bode plot of the loop gain when using a lighting application with LED's operating in constant current mode. Note that it is very important to understand the AC resistance of the LEDs that are being used. Please consult the LED manufacturer for details. For a series string, you should add the individual LED resistances and combine them into one lumped value to simplify the analysis.

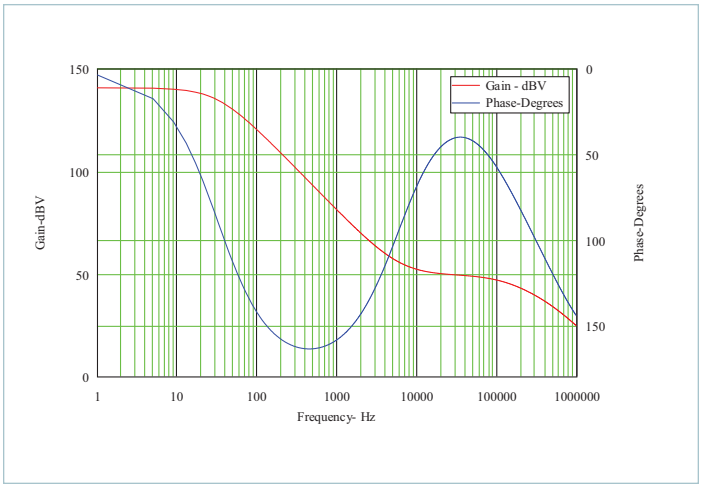


Figure 66 — *$GM_{LGH}(s)$ gain/phase plot compensated*

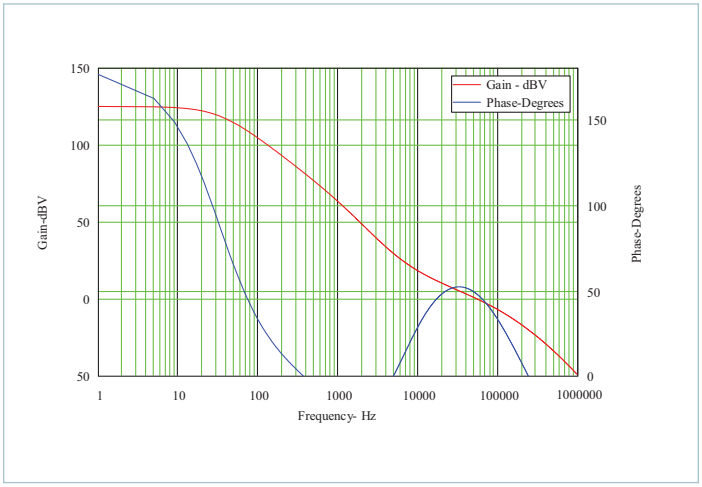


Figure 67 — *Lighting application loop gain/phase plot*

Filter Considerations

The PI354x-00 requires low-impedance ceramic input capacitors (X7R/X5R or equivalent) to ensure proper start up and high-frequency decoupling for the power stage. The PI354x-00 will draw nearly all of the high-frequency current from the low-impedance ceramic capacitors when the main high-side MOSFET(s) are conducting. During the time the MOSFET(s) are off, the input capacitors are replenished from the source. Table 4 shows the recommended input and output capacitors to be used for the PI354x-00 as well as per capacitor RMS ripple current and the input and output ripple voltages. Table 5 includes the recommended input and output ceramic capacitors.

It is very important to verify that the voltage supply source as well as the interconnecting lines are stable and do not oscillate.

Input Filter Case 1; Inductive source and local, external, input decoupling capacitance with negligible ESR (i.e., ceramic type):

The voltage source impedance can be modeled as a series R_{line} L_{line} circuit. The high-performance ceramic decoupling capacitors will not significantly damp the network because of their low ESR; therefore in order to guarantee stability the following conditions must be verified:

$$R_{line} > \frac{L_{line}}{\left(C_{IN\_INT} + C_{IN\_EXT}\right) \bullet \left| r_{EQ\_IN} \right|} \qquad (17)$$

$$R_{line} << \left| r_{EQ\_IN} \right| \qquad (18)$$

Where r_{EQ_IN} can be calculated by dividing the lowest line voltage by the full load input current. It is critical that the line source impedance be at least an octave lower than the converter's dynamic input resistance, Equation 18. However, R_{line} cannot be made arbitrarily low otherwise Equation 17 is violated and the system will show instability, due to an under-damped RLC input network.

Input Filter case 2; Inductive source and local, external input decoupling capacitance with significant $R_{C_{IN\_EXT}}$ ESR (i.e., electrolytic type):

In order to simplify the analysis in this case, the voltage source impedance can be modeled as a simple inductor L_{line}.

$$\left| r_{EQ\_IN} \right| > R_{C_{IN\_EXT}} \qquad (19)$$

$$\frac{L_{line}}{C_{IN\_INT} \bullet R_{C_{IN\_EXT}}} < \left| r_{EQ\_IN} \right| \qquad (20)$$

Notice that the high-performance ceramic capacitors C_{IN_INT} within the PI354x-00 should be included in the external electrolytic capacitance value for this purpose. The stability criteria will be:

Equation 20 shows that if the aggregate ESR is too small – for example by using very high-quality input capacitors (C_{IN_EXT}) – the system will be under-damped and may even become destabilized. As noted, an octave of design margin in satisfying Equation 19 should be considered the minimum.

When applying an electrolytic capacitor for input filter damping the ESR value must be chosen to avoid loss of converter efficiency and excessive power dissipation in the electrolytic capacitor.

VDR Bias Regulator

The VDR internal bias regulator is a ZVS switching regulator that resides internal to the PI354x-00 product family. It is intended strictly for use to power the internal controller and driver circuitry. The power capability of this regulator is sized only for the PI354x-00, with adequate reserve for the application it was intended for. It may be used for as a pull-up source for open collector applications and for other very low-power use with the following restrictions:

1. The total external loading on VDR must be less than I_{VDR}.
2. No direct connection is allowed. Any noise source that can disturb the VDR voltage can also affect the internal controller operation. A series inpedance is required between the VDR pin and any external circuitry.
3. All loads must be locally decoupled using a 0.1µF ceramic capacitor. This capacitor must be connected to the VDR output through a series resistor no smaller than 1kΩ, which forms a low-pass filter.

System Design Considerations

1. *Inductive loads:* As with all power electronic applications, consideration must be given to driving inductive loads that may be exposed to a fault in the system which could result in consequences beyond the scope of the power supply primary protection mechanisms. An inductive load could be a filter, fan motor or even excessively long cables. Consider an instantaneous short circuit through an un-damped inductance that occurs when the output capacitors are already at an initial condition of fully charged. The only thing that limits the current is the inductance of the short circuit and any series resistance. Even if the power supply is off at the time of the short circuit, the current could ramp up in the external inductor and store considerable energy. The release of this energy will result in considerable ringing, with the possibility of ringing nodes connected to the output voltage below ground. The system designer should plan for this by considering the use of other external circuit protection such as load switches, fuses, and transient voltage protectors. The inductive filters should be critically damped to avoid excessive ringing or damaging voltages. Adding a high-current Schottky diode from the output voltage to PGND close to the PI354x-00 is recommended for these applications.
2. *Low-voltage operation:* There is no isolation from an SELV (Safety-Extra-Low-Voltage) power system. Powering low-voltage loads from input voltages as high as 60V may require additional consideration to protect low-voltage circuits from excessive voltage in the event of a short circuit from input to output. A fast TVS (transient voltage suppressor) gating an external load switch is an example of such protection.
3. *Use of Lighting Mode* (LGH) as a battery charger is certainly very feasible. It is fashionable to design these chargers such that the battery is always connected to it. Since the Buck topology is not isolated, shorting the input terminals or capacitors of an unpowered regulator/charger could allow damaging current flow through the body diode of the high-side MOSFET that would be unprotected by a conventional input fuse. It is recommended to connect the PI354x-00 family to the battery using an active ORing device if LGH mode is used as a constant current battery charger. The same should be considered for super-capacitor applications as well.

Device	V_{IN} (V)	I_{LOAD} (A)	C_{INPUT} Ceramic X7R	C_{OUTPUT} Ceramic X7R	C_{INPUT} Ripple Current (A_{RMS})	C_{OUTPUT} Ripple Current (A_{RMS})	Input Ripple (mVpp)	Output Ripple (mVpp)	Transient Deviation (mVpk)	Recovery Time (µs)	Load Step (A) (Slew/µs)
PI3542-00	48	10	5 x 2.2µF 100V	6 x 100µF	0.7	1.32	416	47	±80	40	5 (1A/µs)
		5					220	22			
PI3543-00	48	10	5 x 2.2µF 100V	6 x 100µF	0.8	1.3	464	61.6	±90	40	5 (1A/µs)
		5					230	31			
PI3545-00	48	10	5 x 2.2µF 100V	6 x 47µF	.88	1.37	485	62	±150	40	5 (1A/µs)
		5					245	32			
PI3546-00	48	9	5 x 2.2µF 100V	6 x 10µF	1.12	1.26	880	114	±300	20	5 (1A/µs)
		4.5					125	33			

Table 3 — *Recommended input and output capacitance*

Murata Part Number	Description
GRM32ER72A225KA35	2.2µF 100V 1210 X7R
GRM32EC70J107ME15	100µF 6.3V 1210 X7S:EIA
GRM32ER71A476KE15	47µF 10V 1210 X7R:EIA
GRM32ER61H106MA12	10µF 50V 1210 X5:EIA

Table 4 — *Capacitor manufacturer part numbers*

Layout Guidelines

To optimize maximum efficiency and low-noise performance from a PI354x-00 design, layout considerations are necessary. Reducing trace resistance and minimizing high current-loop returns along with proper component placement will contribute to optimized performance.

A typical buck converter circuit is shown in Figure 68. The potential areas of high parasitic inductance and resistance are the circuit return paths, shown as LR below.

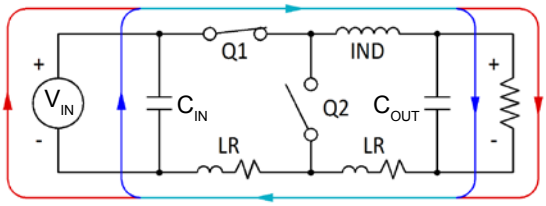


Figure 68 — *Typical Buck regulator*

The path between the C_{OUT} and C_{IN} capacitors is of particular importance since the AC currents are flowing through both of them when Q1 is turned on. Figure 69, schematically, shows the reduced trace length between input and output capacitors. The shorter path lessens the effects that copper trace parasitics can have on the PI354x-00 performance.

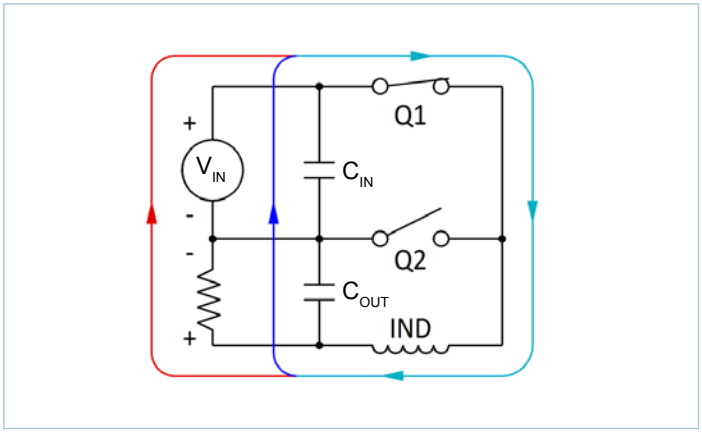


Figure 69 — *Current flow: Q1 closed*

When Q1 is on and Q2 is off, the majority of C_{IN}'s current is used to satisfy the output load and to recharge the C_{OUT} capacitors. When Q1 is off and Q2 is on, the load current is supplied by the inductor and the C_{OUT} capacitor as shown in Figure 70. During this period C_{IN} is also being recharged by the V_{IN}. Minimizing C_{IN} loop inductance is important to reduce peak voltage excursions when Q1 turns off. Also, the difference in area between the C_{IN} loop and C_{OUT} loop is vital to minimize switching and GND noise.

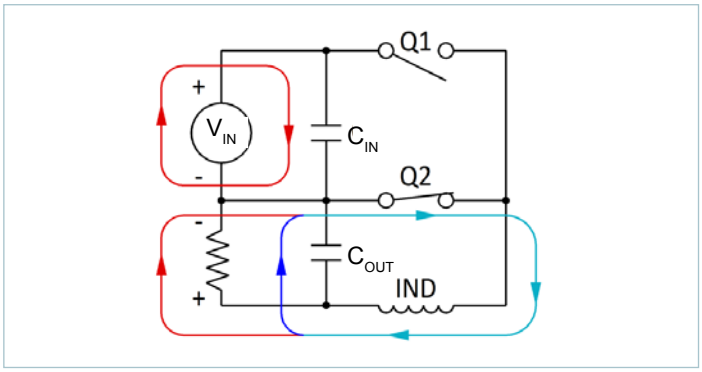


Figure 70 — *Current flow: Q2 closed*

The recommended component placement, shown in Figure 71, illustrates the tight path between C_{IN} and C_{OUT} (and V_{IN} and V_{OUT}) for the high AC return current. This optimized layout is used on the PI354x-00 evaluation board.

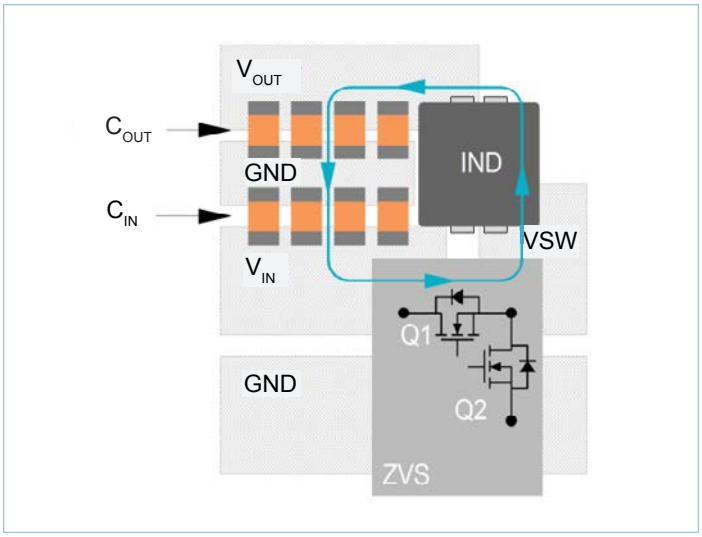
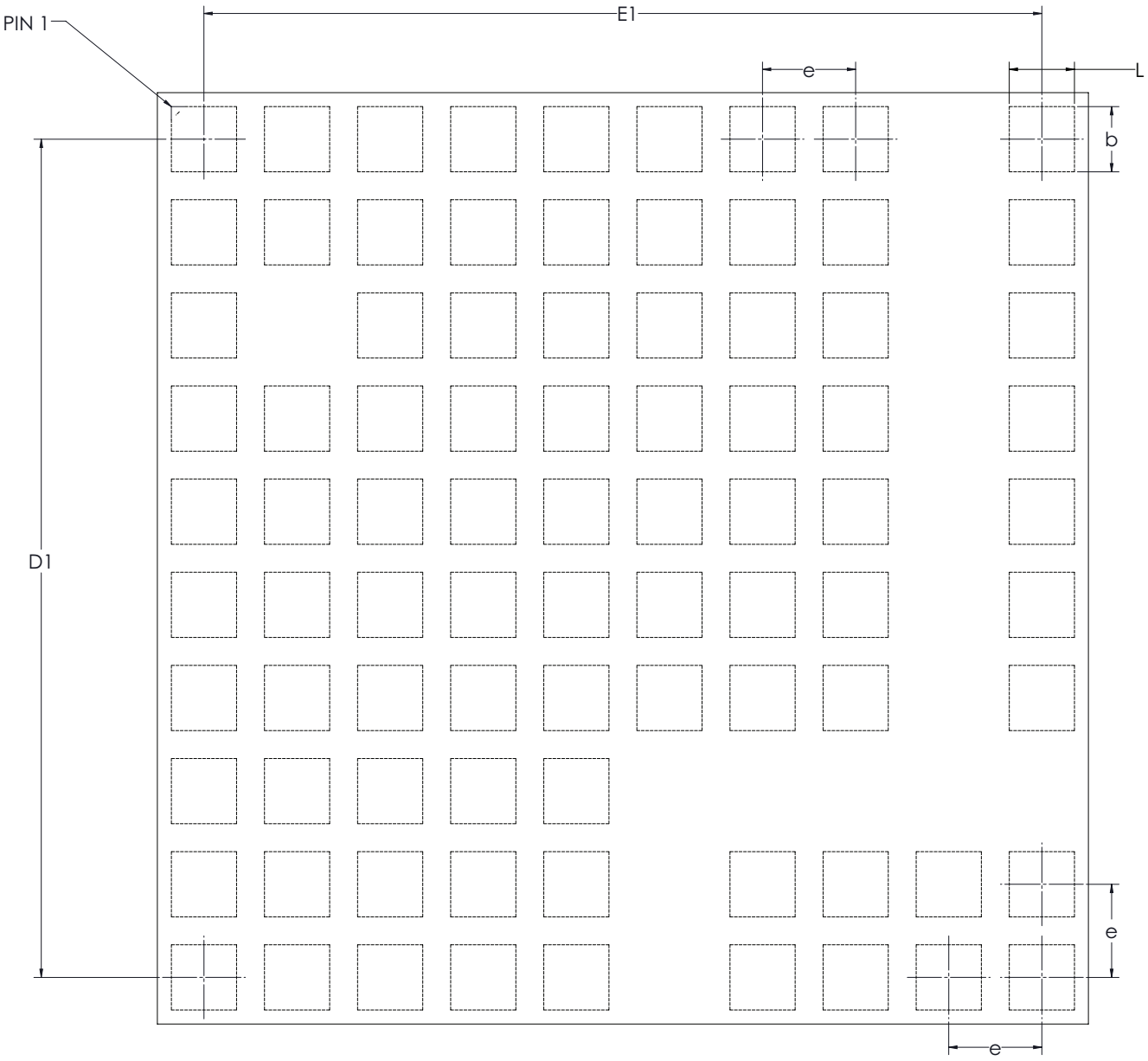


Figure 71 — *Recommended component placement and metal routing*

Recommended PCB Footprint and Stencil

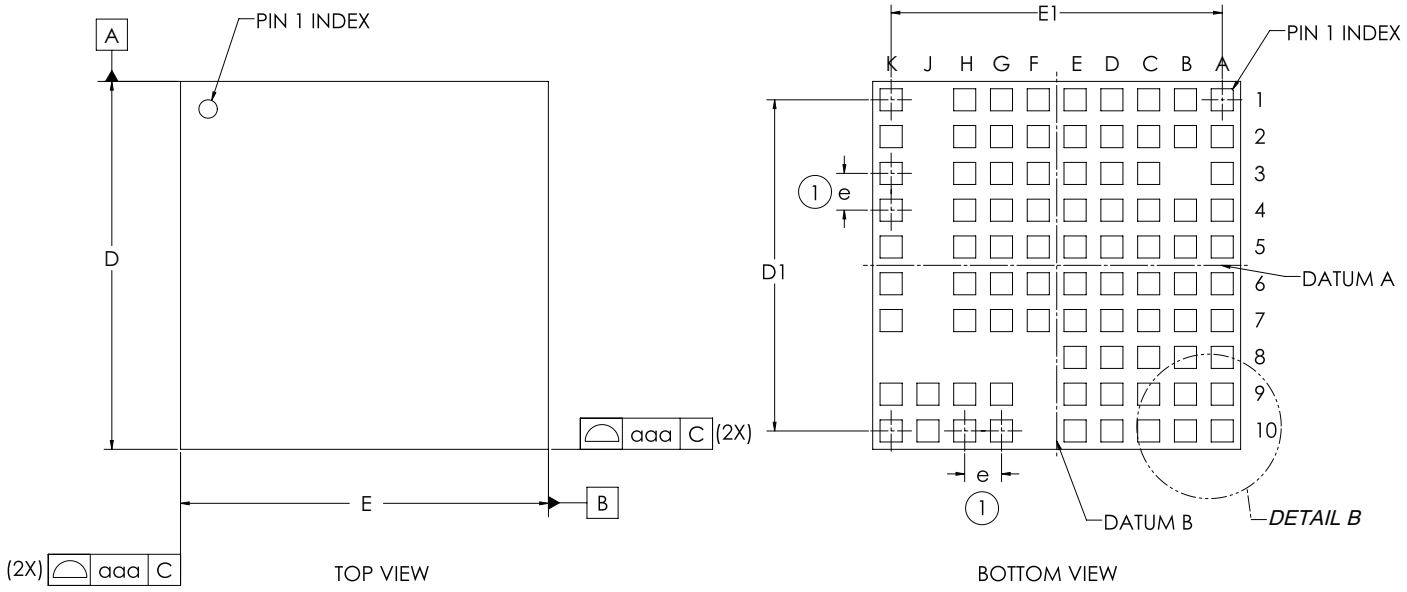


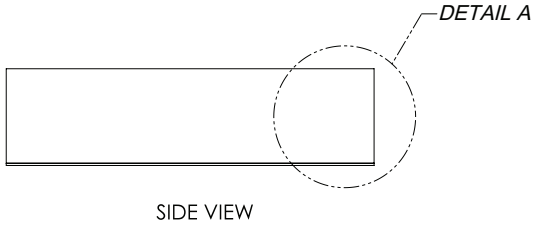
PCB LAND PATTERN
PI354X

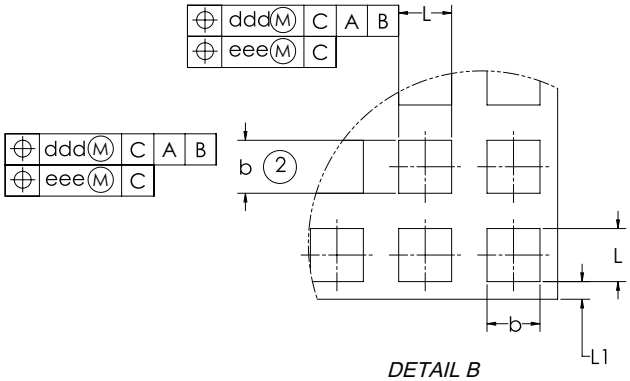
DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
b & L	0.50	0.55	0.60
D1		9.00 BSC	
E1		9.00 BSC	
e		1.00 BSC	

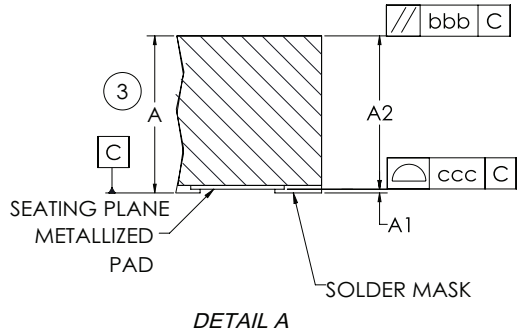
The recommended receiving footprint for PI354x-00 10mm x 10mm package. All pads should have a final copper size of 0.55mm x 0.55mm, whether they are solder-mask defined or copper defined, on a 1mm x 1mm grid. All stencil openings are 0.45mm when using either a 5mil or 6mil stencil.

LGA Package Drawings







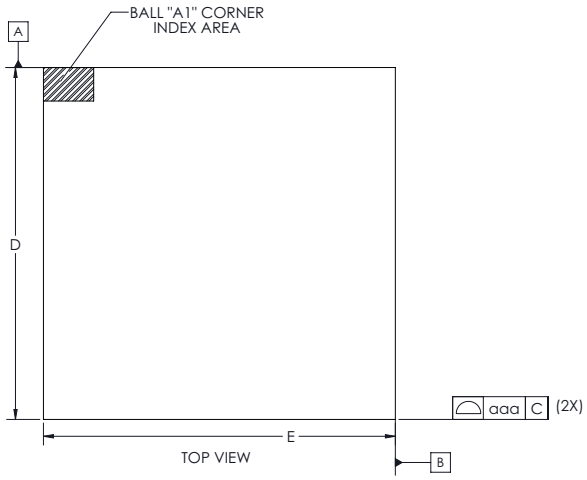


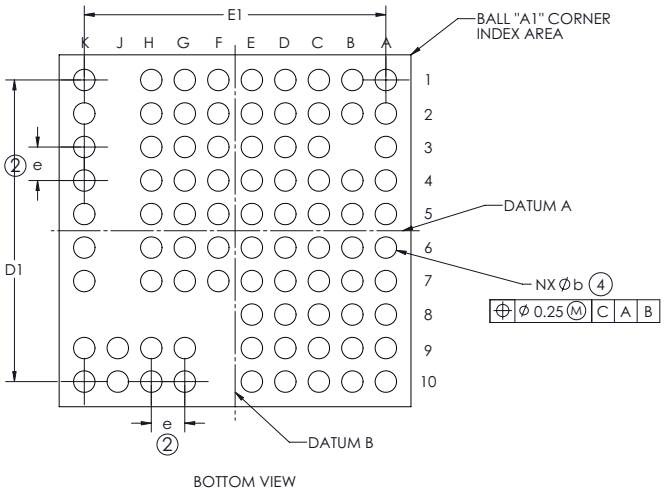
REF.	TOLERENCE OF FORM AND POSITION
aaa	0.10
bbb	0.10
ccc	0.08
ddd	0.10
eee	0.08

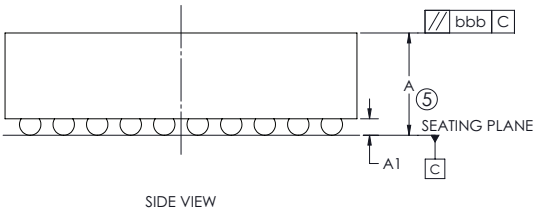
PI354x			
REF	Min.	Nom.	Max.
A	2.49	2.56	2.63
A1	-	-	0.04
A2	-	-	2.59
b	0.50	0.55	0.60
L	0.50	0.55	0.60
D		10.00 BSC	
E		10.00 BSC	
D1		9.00 BSC	
E1		9.00 BSC	
e		1.00 BSC	
L1	0.175	0.225	0.275

NOTES:
1. 'e' REPRESENTS THE BASIC TERMINAL PITCH. SPECIFIES THE GEOMETRIC POSITION OF THE TERMINAL AXIS.
2. DIMENSION 'b' APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.00mm AND 0.25mm FROM TERMINAL TIP.
3. DIMENSION 'A' INCLUDES PACKAGE WARPAGE.
4. EXPOSED METALLIZED PADS ARE CU PADS WITH SURFACE FINISH PROTECTION.
5. ALL DIMENSIONS ARE IN MM UNLESS OTHERWISE SPECIFIED.
6. RoHS COMPLIANT PER CST-0001LATEST REVISION.

BGA Package Drawings







NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
② 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. 'M' REPRESENTS THE BASIC SOLDER BALL MATRIX SIZE. AND SYMBOL 'n' IS THE NUMBER OF BALLS AFTER DEPOPULATING.
④ 'b' IS MEASURABLE AT THE MAXIMUM SOLDER BALL DIAMETER AFTER REFLOW PARALLEL TO PRIMARY DATUM C .
⑤ PRIMARY DATUM C AND SEATINGPLANE ARE DEFINED BY THE SPERICAL CROWNS OF THE SOLDER BALLS.
6. PACKAGE SURFACE SHALL BE MATTE FINISH CHARMILLES 24 TO 27.
7. SUBSTRATE MATERIAL BASE IS BT RESIN.
8. THE OVERALL PACKAGE THICKNESS "A" ALREADY CONSIDERS COLLAPSE BALLS
9. DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.
10. RoHS COMPLIANT PER CST-0001 LATEST REVISION.

DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
A	2.96	3.05	3.14
A1	0.44	0.49	0.54
D		10.50	
D1		9.00 BSC	
E		10.50	
E1		9.00 BSC	
b	0.59	0.64	0.69
aaa		0.20	
bbb		0.25	
e		1.00 BSC	
M		10	
n		85	

Revision History

Revision	Date	Description	Page Number(s)
1.0 - 1.1	05/2015	Released Engineering format/style	n/a
1.2	10/12/15	Reformatted in new template	n/a
1.3	02/19/16	Updated PCB Footprint	34
1.4	05/09/16	Typo correction Correction to Conditions on Switching Frequency Updated Input OVLO Threshold TRK function performance enhancement Updated package drawing	7 & 25 8 8, 12, 16 & 20 9, 13, 17 & 21 35
1.5	11/08/16	Features and Applications Lists Updated LGH Reference Max changed from 105 to 107mV Input Quiescent Current Performance improved EN section moved to common electrical specifications on pg 7 & removed from individual product electrical specifications. Table 4 Capacitor Part Numbers updated Package Outline Drawing updated	1 7 8, 12, 16 & 20 7, 9, 13, 17 & 21 34 36
1.6	03/09/17	Amendments to Absolute Maximum Ratings Clarifications to Enable, Protection and Soft Start, Tracking and Error Amplifier Package drawings updated Corrections to Figures 49, 50, 51 Updated Overtemperature Protection Output Voltage Set Point description updated Equations amended	4 8, 10 6, 36, 37 25, 26, 27 26 27 27, 31, 32
1.7	08/08/18	Updated land pattern and LGA package drawing Added BGA package information	36, 37 38
1.8	09/14/18	Correction to BGA height measurement	1
1.9	03/03/20	Update to Equation 6	29
2.0	05/15/20	Updated to add recommended Pulse Electronics inductors	27
2.1	08/11/20	Updated terminology	27
2.2	10/30/20	Added ESD specification	3

Please note: one page added in Rev 1.6, 1.7.

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