WiLink™ Module Hardware Integration Guide

This document provides the necessary *Bluetooth*®/Bluetooth low energy and WLAN hardware operation information to aid in system design. This is a review of the integration process of TI's WiLink Module into final product PCB. When designing your own system around the TI module, it is recommended to step through the guidelines outlined below.

- WL18xxMOD product page [1]

NOTE: You can check your TI module WL18XXMOD design to PCB integration with the WL18XXMOD series of easy-to-follow excel Checklist.

Contents

List of Figures

List of Tables

Trademarks

1 Module Variant Table

Table 1. WL18XXMODGB (2.4 GHz only module variants)

Device	Reduced integration interfaces Compared to the Main 1835 Module	WLAN 2.4-GHz SISO	WLAN 2.4-GHz MIMO	WLAN 2.4-GHz MRC	Bluetooth
WL1835MOD	• Full version (all of the integration checklist must be applied)	✓	✓	✓	✓
WL1831MOD	• Only the main RF antenna, ANT1 is used and the second one should be left N.C.	✓			✓
WL1805MOD	• For Bluetooth IP removal. Bluetooth EN line must be connected to VSS. Bluetooth HCI, PCM and logger lines should be left N.C.	✓	✓	✓	
WL1801MOD	• Only the main RF antenna, ANT1, is used and the second one should be left N.C. • For Bluetooth IP removal. Bluetooth EN line must be connected to VSS. Bluetooth HCI, PCM and logger lines should be left N.C.	✓			

Table 2. WL18X7MODGI (2.4 GHz and 5 GHz modules)

Device	Redundant Capabilities Compared to the Main 1837 Module	WLAN 2.4-GHz SISO (1)	WLAN 2.4-GHz MIMO (2)	WLAN 2.4-GHz MRC (3)	Bluetooth	WLAN 5-GHz SISO
WL1837MOD	• Full version (all of the integration checklist must be applied)	✓	✓	✓	✓	✓
WL1807MOD	• For Bluetooth IP removal: Bluetooth EN line must be connected to VSS. Bluetooth HCI, PCM and logger lines should be left N.C.	✓	✓	✓		✓

(1) Single input, single output (SISO)

(2) Multiple input, multiple output (MIMO)

(3) Maximum ratio combining (MRC)

NOTE: Customers working with WL1837MOD/WL1807MOD modules that require only the single antenna solution (2.4 Ghz WLAN SISO/ Bluetooth/ 5 GHz single antenna), while reusing the original certification, can do so by making sure that no RF comes out of the second antenna port (2.4 MIMO only / 5 Ghz diversity). To do this, use the following requirements:

- Leave the second module RF port open (pin number 18 = N.C.)
- In the WL1837MOD INI, make sure that only 1 antenna is selected for 2.4 GHz by setting parameter NumberOfAssembledAnt2_4 = 1;

1.1 WiLink WLAN Antenna Configuration

1.1.1 Single-Input Single-Output (SISO)

SISO is an acronym for single-input and single-output system. SISO technology use of only one antenna both in the transmitter and receiver side.

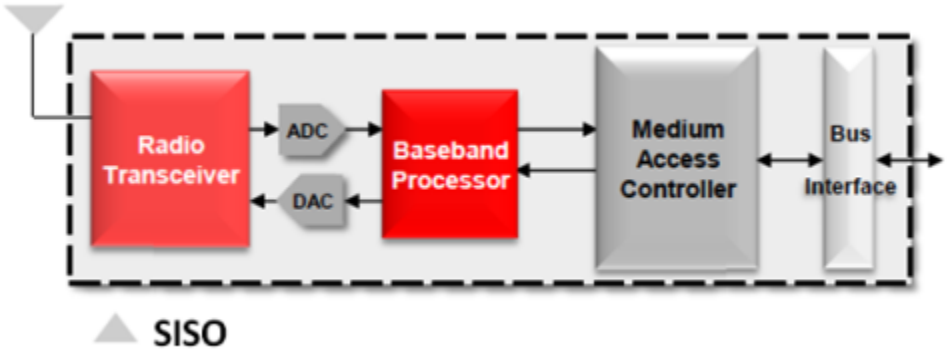


Figure 1. SISO

1.1.2 Multiple-Input Multiple-Output (MIMO)/Maximum Ratio Combining (MRC)

MIMO is an acronym for multiple input multiple output. This technology can multiply the throughput capacity by delivering multiple data streams over multiple antennas.

MRC is an acronym for maximum ration combining, This technology enables diversity of the reception signal, done by combining the signal received in each antenna with the proper gain factor according to its quality.

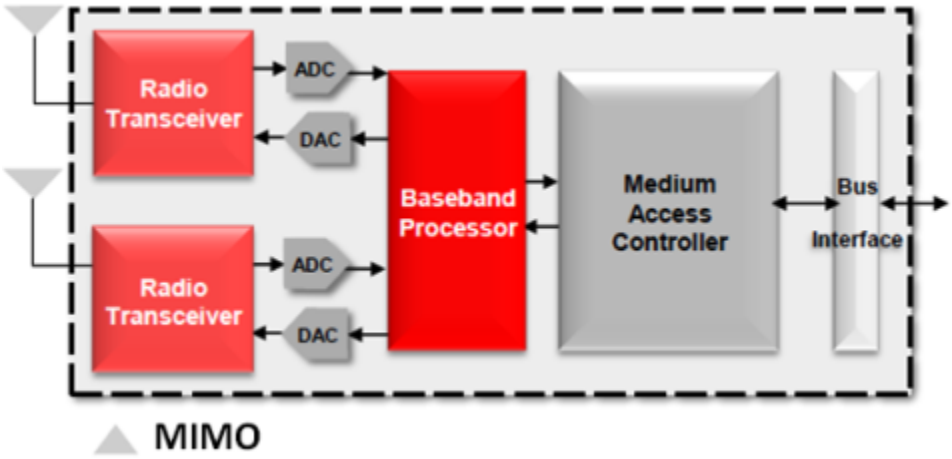


Figure 2. MIMO

2 Critical Connections

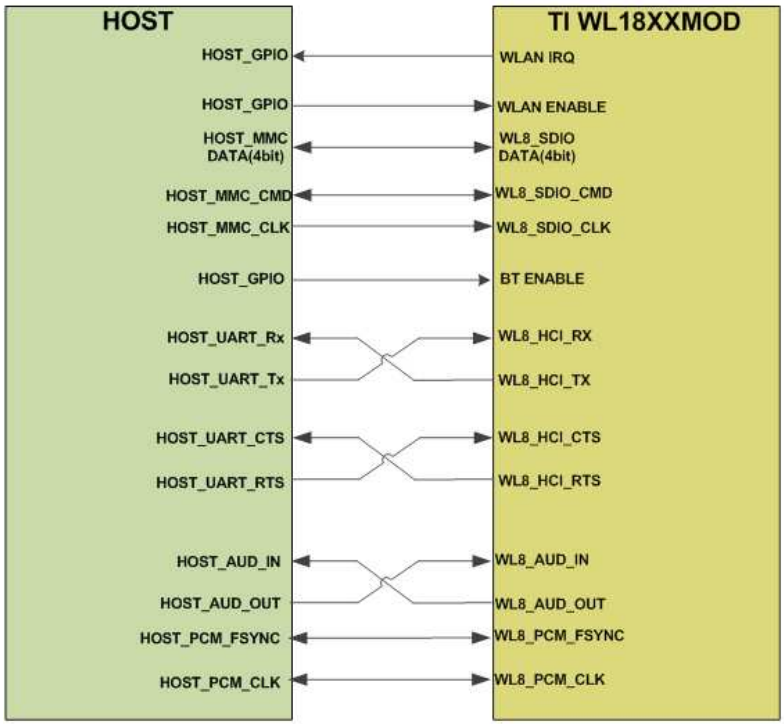


Figure 3. IO Connection Operational Mode

NOTE: The reference is built using AM335 processor integration. For some of the other processors, the RTS/CTS, TX/RX lines can be routed directly.

3 Power Supply

3.1 Power Up/Shutdown Sequence

Make sure the power up and shutdown sequence is kept at all times.

Table 3. Supply Lines

Pin No	Name	Description
40	WL_EN	WLAN enable line from system
41	BT_EN	Bluetooth enable line from system
36	SCLK	Slow clock is running at 32 kHz
46,47	VBAT	VBAT is high and stable at approximately 3.3 V
38	VIO	VIO is high and stable at approximately 1.8 V

3.1.1 Power Up

To power up, do the following:

1. Ensure slow clock, V_{IO}, and V_{BAT} are stable.
2. Assert BT_EN or WL_EN high.

Internal DC2DCs, LDOs, and clocks start to ramp and stabilize.

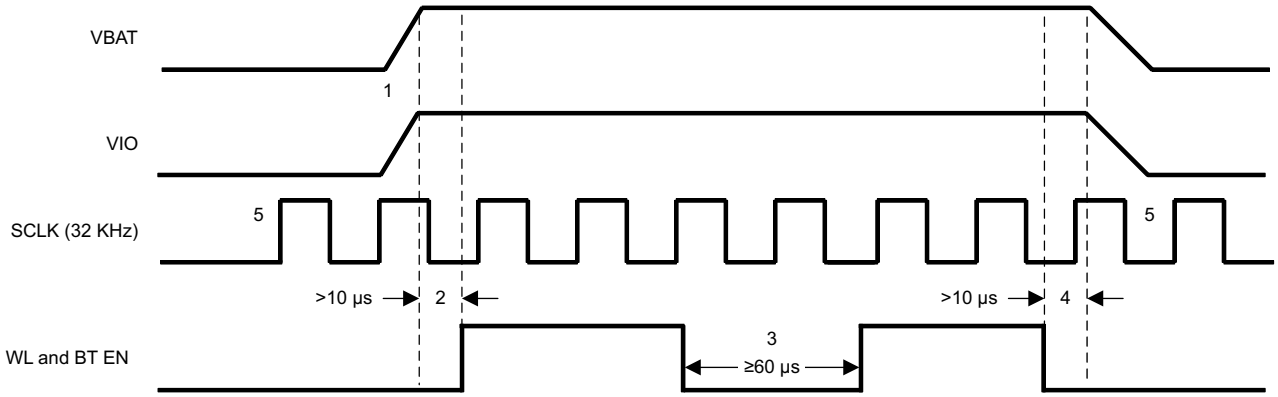
3.1.2 Shutdown

Shutdown

1. Ensure the supplies to the device (V_{BAT}, V_{IO}, and slow clock) are stable and available.
2. De-assert BT_EN and WL_EN.
3. De-assert the supplies to the chip (V_{BAT} and V_{IO})

3.2 Power Sequencing

The most crucial points during integration of the WiLink Module is that proper power-up and power-down sequences must be followed in order to avoid damage to the device.



(1) On system level, either V_{BAT} and V_{IO} can come up first.

(2) V_{BAT} supplies, V_{IO} supplies, and slow clock (SCLK) msut be enabled before EN is asserted and at all times when EN is active.

(3) Keep a 60-µs delay between two consecutive device enables. The device is assumed to be in a shutdown state during that period; all enables to the device are low for that minimum duration.

(4) Deassert the enable line at least 10 µs before the V_{BAT} or V_{IO} can be lowered. (The order in which supplies are turned off after EN shutdown in immaterial).

(5) The SCLK I/O cell is a fail safe; the clock can be supplied before the V_{BAT} and V_{IO} supplies.

Figure 4. Power Sequencing

4 Clocks

4.1 Slow Clock

- The slow clock must be a free-running 32.768 KHz digital square wave
- The slow clock should be connected to pin 36 of the module
- Verify that the voltage range is between 0 V-1.8 V

4.2 Fast Clock

The WL18xxMOD uses a dedicated on-board 26 MHz fast clock TCXO.

5 Current Consumption

The power supplies for Vbat and VIO must handle the maximum current loads incurred by the WL18xx.

Please verify that your power supply can handle the maximum loads listed in Table 4 for each subsystem.

Table 4. Recommended Current Requirement

Parameter	Power Supply Required Current	Typical Values	Units
WLAN SISO or MIMO 2.4 GHz, 5 GHz SISO/MRC, Bluetooth	VBAT (1)	1	A
WLAN SISO and Bluetooth	VBAT (1)	750	mA
VIO	VIO (2)	200	mA

(1) VBAT current is based on calibration current as well as maximum TX currents from all IPs

(2) VIO current requirement takes into account slow clock supply and LS, which are powered with the same supply from the WL8 side.

5.1 Performance Parameters - Typical

- System design power scheme must comply with both peak and average TX bursts
- WLAN maximum VBAT current draw of 725 mA with MIMO continues burst configuration
- Peak current VBAT can hit 850 mA during device calibration (1)

(1)
- At wakeup, the WiLink™ 8 module performs the entire calibration sequence at the center of the 2.4-GHz band.
- Once a link is established, calibration is performed periodically (every 5 minutes) on the specific tuned channel.
- The maximum VBAT value is based on peak calibration consumption with a 30% margin.

For more information on WiLink8 current consumption and Max VBAT / VIO, see the WL18xxmod device-specific data sheet (http://www.ti.com/lsds/ti/wireless_connectivity/wilink/products.page).

6 Antenna

This device is intended only for OEM integrators under the following conditions:

- The antenna must be installed so that 20 cm is maintained between the antenna and users.
- The transmitter module cannot be co-located with any other transmitter or antenna.
- The radio transmitter can operate only using an antenna of a type and maximum (or lesser) gain approved by TI. Table 5 lists the antennas approved by TI for use with the radio transmitter along with maximum allowable gain values. Antenna types not included in the list or having a gain greater than the maximum indicated are strictly prohibited for use with this transmitter.

Table 5. Approved Antenna Types and Maximum Gain Values

Antenna Type	Brand	2.4 GHz	4.9 to 5.9 GHz (1)	Unit
PCB	Ethertronics	–0.600	4.50	dBi
Dipole	LSR	2.00	2.00	
PCB	Laird	2.00	4.00	
Chip	Pulse	3.20	4.20	
PIFA	LSR	2.00	3.00	
Chip	TDK	2.27	3.96	

(1) Range is approximate.

NOTE: If these conditions cannot be met (for example, with certain laptop configurations or co-location with another transmitter), the FCC/IC authorization will not be considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator is responsible for reevaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

- It is suggested to place a Pi matching network place holder before the antenna on board

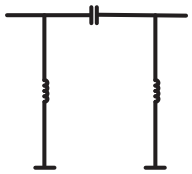


Figure 5. Antenna Matching Network in PI Configuration

- It is strongly advised to have a debug miniature connector on the PCB
- Switching between the antenna and the debug connector should be done in RNR configuration to avoid stubs

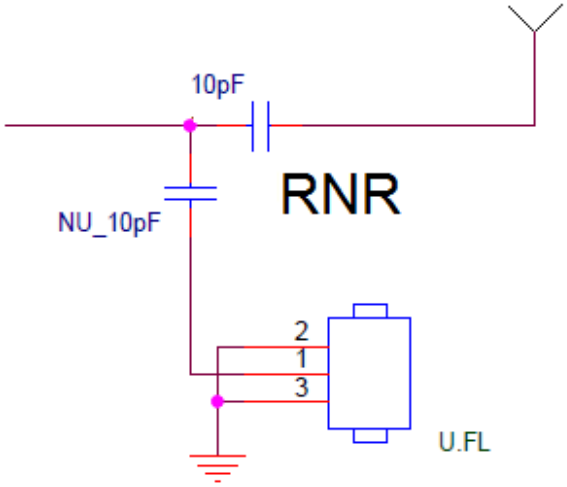


Figure 6. RNR Configuration

- Antenna should be placed away from the rest of the circuit
  - Avoid digital and analog routing in the area, metal enclosure.
- MIMO antenna spacing
  - Distance between the two antennas is advised to be greater than half of the wavelength (62.5 mm at 2.4 GHz)

7 Ground Connections

All the ground pins of the module must be connected to ground on the main PCB.

8 Layout

For more information, see the WL1837 User's Guide [5].

9 Hardware Troubleshoot

This section is intended to cover the basic hardware troubleshoot that you may come across bringing up the WL18xxMOD on the final board; the device has several interfaces and sequences that must be kept in order to operate the device in properly.

9.1 System Requirements

For basic integration, the process requires the following components:

- Wireless Tool Package located at TI.COM
- Minimum requirements: PC running Pentium II
- Operating systems: Windows 2000, Windows XP, Windows 7
- Serial communication port (RS-232) or USB port with UART-to-USB adapter (to enable the RS232 interface on the WiLink 8.0 IC)
- Access to WL_UART_DBG pin
- Access to BT_UART_DBG
- Access to RS232 Tx , RS232 Rx Pins
  - HCI UART Pins
- Oscilloscope
- Multimeter

Debug and calibration tools for WLAN and Bluetooth require four UART ports. The most efficient way to drive these ports to the PC is to use a UART-to-USB converter (not included in the wireless tools package). TI recommends using the WL18XXCOM82SDMMC SDMMC-to-COM8 adapter with the TI WL1837MODCOM8I module or the WL1835MODCOM8B module on the COM8 board.

NOTE: Multiple UART-to-COM8 adapters are available on the market, such as the FTDI Chip development modules.

9.2 Power Rails

There are two power rails that must feed into the WiLink system:

- VBAT - Main power supply source (typically 3.3 V - 3.6 V)
  - VBAT should be connected to pin 46 and 47 of the module
- VIO - Voltage reference from host (1.8 V)
  - VIO should be connected to pin 38 of the module
  - Can be used for Level shifter supply and slow clock OSC supply

9.3 Critcal Supplies

Make sure all of the critical supplies are in the range of the following expected values:

Table 6. Critical Supplies

Pin No	Name	Description	Frequency [Hz]	Amplitude [V]	Current [mA]
–	DC_IN	Depends on the system			
36	Slow Clock	External 32 kHz slow clock	32K	1.8	–
46,47	VBAT	DC supply range for all modes	–	3.3-3.6	1000
38	VIO	I/O ring power supply voltage	–	1.8	200

1. VBAT and VIO amplitude and current are maximum values.

9.4 Sense on Reset

Wilink8 has several wake-up options that are entered through sense on reset by three IO's of the device: IRQ_WL, UART_DBG_BT, AUD_OUT_BT.

Once Bluetooth or WLAN enable bit is set to high, the device checks the state of the lines and wakes up in that specific mode.

There are only two modes or configurations that are supported by the device, all of the rest are prohibited and the user must verify that there is no option on the system level to enter the prohibited modes.

The supported modes are:

- Operational mode:
  - IRQ_WL = 0, UART_DBG_BT = 1, AUD_OUT_BT = 0

    Operational mode is set by default using internal pull of WiLink (90K typical).
- Debug mode:

  WLAN RS232 debug interface and Jtag interface are muxed out to the WiLink IO's by default, nevertheless, this mode is only for debug a 10K resistor pull up place holder on the IRQ line should be placed. It can be applied only in case the debug mode is required:
  - IRQ_WL = 1, UART_DBG_BT = 1, AUD_OUT_BT = 0

NOTE: In order to avoid an undefined state of the device, be extremely careful when level-shifting those three I/Os to ensure that only those one of the two supported configurations of the device are applied.

For further details, see *Level Shifting WL18xx I/Os* (SWRA448).

9.5 WLAN

9.5.1 WLAN Host Interface (SDIO)

The SDIO is the host interface for WLAN. The interface between the host and the WiLink module uses an SDIO interface and supports a maximum clock rate of 52 MHz.

The device SDIO also supports the following features of the SDIO V3 specification:

- 4-bit data bus
- Synchronous and asynchronous in-band interrupt
- Default and high-speed (HS, 52 MHz) timing
- Sleep and wake commands
- The WLAN subsystem is controlled via an SDIO interface. The WLAN acts as a slave with the processor as host. The host should generate the SDIO clock and read/write from the WLAN interface.
- Verify that the SDIO bus pins are connected to the host. These pins include:

Table 7. SDIO Interface Lines

Pin Number	Name	Type	Description
6	SDIO_CMD	I/O	SDIO command line. This is a bidirectional line. The host sends commands and the WLAN responds to these commands.
8	SDIO_CLK	I	SDIO clock input line. This line is generated by the host.
10	SDIO_D0	I/O	SDIO data 0 line. This is the primary data line used in both 1-bit and 4-bit SDIO mode. This is a bidirectional line.
11	SDIO_D1	I/O	SDIO data 1 line. This is one of four data lines. This line is used only in 4-bit mode. This is a bidirectional line.
12	SDIO_D2	I/O	SDIO data 2 line. This is one of four data lines. This line is used only in 4-bit mode. This is a bidirectional line.
13	SDIO_D3	I/O	SDIO data 3 line. This is one of four data lines. This line is used only in 4- bit mode. This is a bidirectional line.
14	WLAN_IRQ	O	Generates interrupt from the WLAN chip toward the HOST. It is used to signal the HOST on many events like received data from the WLAN media is ready at the firmware (WLAN Chip) queue, the last Tx frame that was transmitted, all kind of asynchronous messages (evens), and so on.
40	WLAN_EN	I	WLAN enable signal, should be "1" in order enable the WLAN operation, once the WLAN enable signal is "0" the WLAN part of the chip is reset in a way that the firmware has to be loaded again after enabling the WLAN.

- Host must provide PU using a 10-K resistor for all non-CLK SDIO signals.
- In order to follow the wakeup/shutdown requirements, the WL_EN (pin number 40) should be connected to host GPIO. Must be pulled high for WLAN operation. This GPIO should have internal pull-up allowing the WiLink pin to remain high on host suspend. In order to enable WOW feature, a pull up on the line is required during HOST shutdown.
- IRQ_WL should be connected to host GPIO. This GPIO should be able to wake the host from suspend, therefore it's better to always connect the pin (number 14) to the always on domain of the Host. The IRQ_WL pin serves as interrupt generation from WiLink to the host.

NOTE: It is recommended to connect the SDIO directly to the 1.8 V SDIO interface on the host side. In case Level Shifter is inevitable, see *Level Shifting WL18xx I/Os Application Report* (SWRA448).

9.5.2 WLAN IRQ Operation (SDIO Out-of-Band Interrupt)

The WLAN IRQ is an out-of-band interrupt request line that is not defined by the SDIO standard specification. Therefore, a good understanding on how it works is required in order to work with the WL8xx solution.

The WLAN_IRQ line operates as follows:

- The default state of the WLAN_IRQ prior to device enable is internal 100K pulldown (in case of a debug mode there is external 10K pull up)
- After the enable line is applied high, the WL_IRQ is changed to drive logic '0'.
- During firmware initialization, the WLAN_IRQ is configured by the SDIO module.
  - The WLAN firmware creates an interrupt-to-host request, indicated by a 0-to-1 transition on the WLAN_IRQ line (the host must be configured as active high or rising-edge detect).
  - After the host is available, depending on the interrupt priority and other host tasks, it masks the firmware interrupt. The WLAN_IRQ line returns to 0 (a 1-to-0 transition on the WLAN_IRQ line).
  - The host reads the internal register status to determine the interrupt sources. The register is cleared after the read.
  - The host processes all the interrupts read from this register in sequence.
  - The host unmasks the firmware interrupts.
- The host is ready to receive another interrupt from the WLAN device.

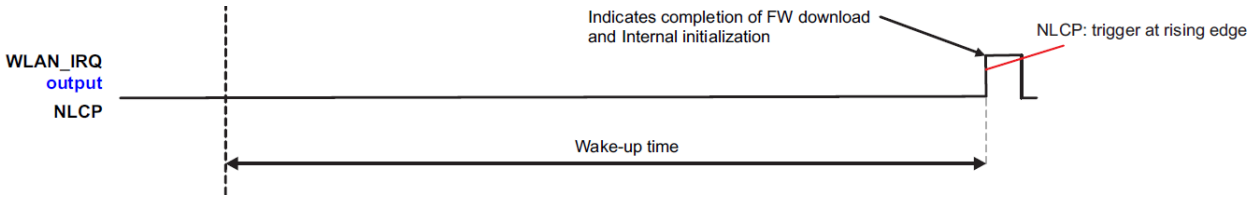


Figure 7. WLAN_IRQ Signal on System Wake Up

For more details on the Wake on Wlan feature, see [3].

9.6 Bluetooth and Bluetooth Low Energy

9.6.1 Bluetooth UART HCI Interface

- The Bluetooth subsystem is controlled via an HCI 4-wire UART interface (H4).
- Verify that the HCI interface is connected as shown in Figure 8. Note that a TX pin always routes to a RX pin, and a RTS pin always routes to a CTS pin.

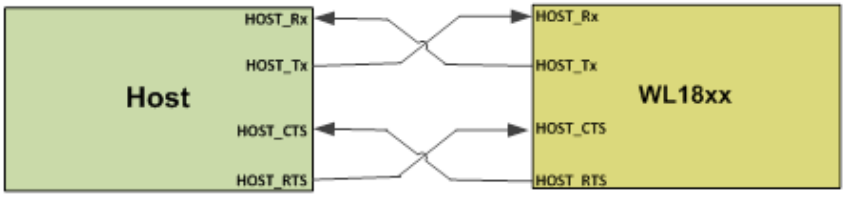


Figure 8. HOST HCI UART Interface

Table 8. HCI UART Interface Lines

Pin Number	Name	Type	Description
41	BT_EN	I	Bluetooth Enable
50	BT_HCI_RTS	O	Bluetooth HCI UART request to send output
51	BT_HCI_CTS	I	Bluetooth HCI UART clear to send input
52	BT_HCI_TX	O	Bluetooth HCI UART transmit output
53	BT_HCI_RX	I	Bluetooth HCI UART receive input

- FUNC1_BT should be NC.
- FUNC2_BT should be NC.

NOTE: In the AM335x integration reference, the RTS and CTS lines are crossed, as shown. For some of the other processors, the RTS/CTS lines must be connected directly.

- In case of host processor I/O is at 3.3 V, use a standard 245 level shifter and not a direction sensing one. For more information, see *Level Shifting WL18xx I/Os* (SWRA448).
- Once Bluetooth EN is asserted to high the Bluetooth FW stored in ROM start to execute, during this time the RTS is driven high to prevent HCI transaction and not to interfere with device boot, once the FW finish the boot process RTS line goes low after approximately 100 mS.

  If logger is configured at this point, WiLink should print boot up message.

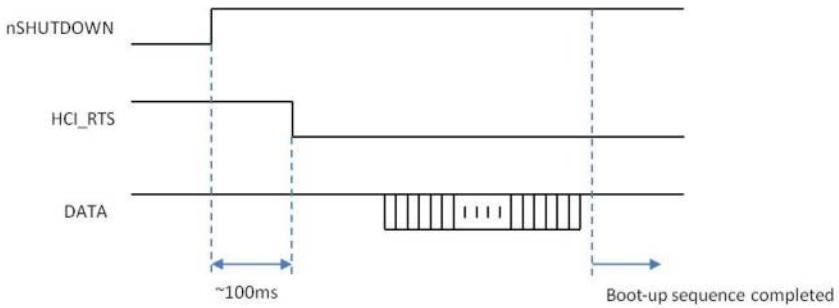


Figure 9. Bootup Sequence Complete

- Connect HCI Tester and Set Baud Rate - 115200, Data Bits - 8, Stop bits -1, Parity - none, Flow Control - HW. On this port, send basic HCI commands (BD Address) to verify connectivity.
- In case UART lines are not operating, make sure that the CTS line is set to 0 on the PC side - the signal on the WiLink Rx input line that comes from the PC (on the port Probe).

  For every packet on Rx, there should be a response on the Tx line from WL18xx.

9.6.2 Bluetooth PCM

There are two lines that can be bidirectional (CLK/FSYNC) to support master and slave configuration and two directional pins: AUD_OUT (output) and AUD_IN (input).

All four lines should be connected to the HOST PCM interface.

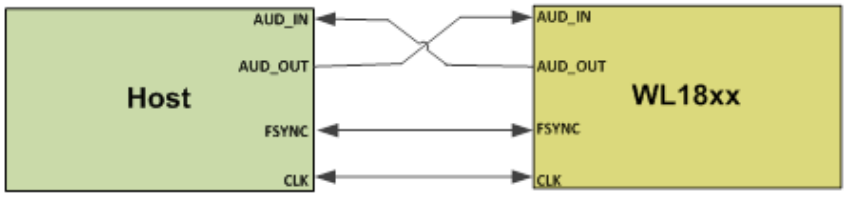


Figure 10. HOST PCM Interface

In case the PCM interface is not used, leave not connected (N.C.).

Table 9. PCM Interface Lines

Pin Number	Name	Type	Description
56	BT_AUD_IN	I	Bluetooth PCM data output
57	BT_AUD_OUT	O	Bluetooth PCM data output
58	BT_AUD_FSYNC	I/O	Bluetooth PCM frame sync input or output
60	BT_AUD_CLK	I/O	Bluetooth PCM clock input or output

9.7 Reserved Pins

- Reserved 1, 2, 3, can be used for Audio sync otherwise, leave N.C.
- GPIO 9, 10, and 12 can be used for ZigBee coexistence
  - GPIO11 can be used for Audio sync, otherwise, leave N.C.

9.8 Debug

Table 10. Debug/RS232 Interface Lines

Pin Number	Name	Type	Description
26	WLAN RS232 RX	I	WLAN debug interface
27	WLAN RS232 TX	O	WLAN debug interface
42	WL_UART_DBG	O	WLAN FW logger
43	BT_UART_DBG	O	BT FW logger

For bring up and evaluation of the module, the following should be connected:

- Pin out GPIO1 and GPIO2 for WLAN RS232 interface to enable RTTT tool for controlling RF test in the absence of a host.
- There is a need to pull up WL_IRQ (10k pull up) at power-on to enable this RS232 UART interface.
- WLAN logger must have at least a TP to allow Wi-Fi Firmware logs to be captured by gLogger. Requires a 1.8 V LVCMOS to USB cable for capture.

- Bluetooth logger must have at least a TP to allow Bluetooth Firmware logs to be captured by gLogger. Requires a 1.8 V LVCMOS to USB cable for capture.
- WLAN RS232 lines - Check transmission on Rx/Tx line, for every packet on Rx should be a response in Tx.

10 WiFi_Zigbee Coex

- For Zigbee/WiFi Coexistence, the following should be connected:

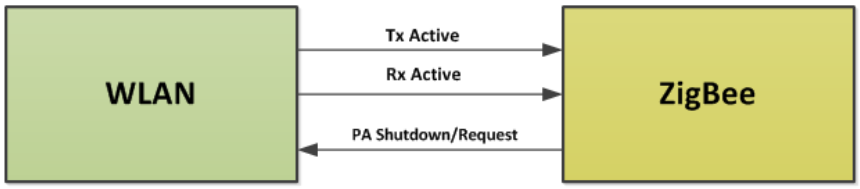


Figure 11. WLAN ZigBee Coexistence

Table 11. WLAN ZigBee Coex Lines

Signal Name	WL18xxMOD IO (1.8 Bv)	CC2530 Zigbee IO (3.3 V)	Direction
Tx Active	GPIO12 (Pin 5)	P1_7 (Pin 37)	From WLAN
Rx Active	GPIO10 (Pin 4)	P0_0 (Pin 19)	From WLAN
PA SHUTDOWN/REQUEST	GPIO9 (Pin 3)	P1_6 (Pin 38)	To WLAN

- For signals level shifting between WL18XXMOD and CC2530, TI recommends the TXS0102 Bidirectional Voltage-Level Translator.

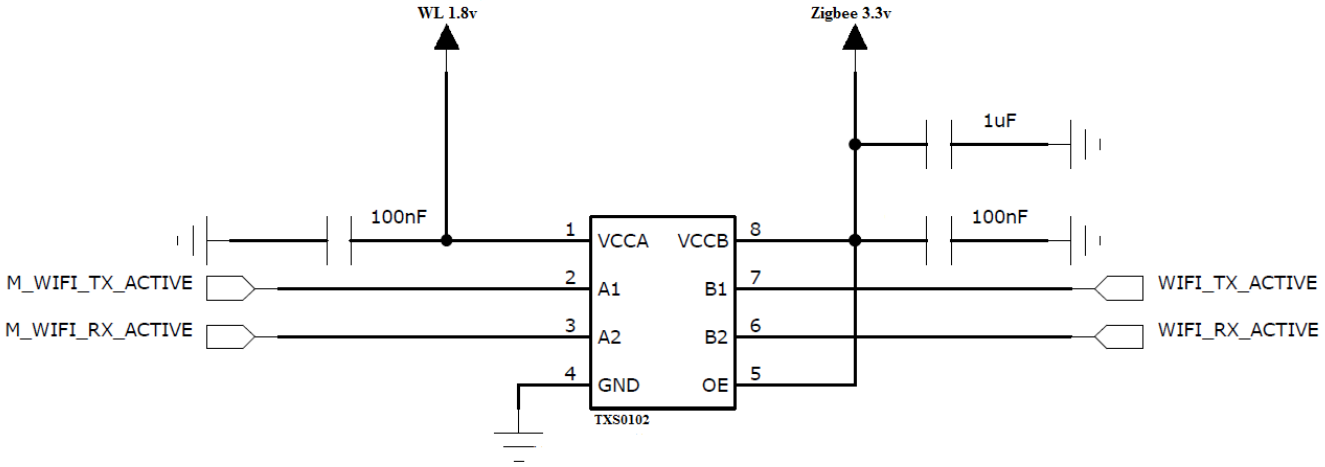


Figure 12. Zigbee_LS

- For the TX disable, one of the options is to use resistor divider or use single bit Level Shifter.

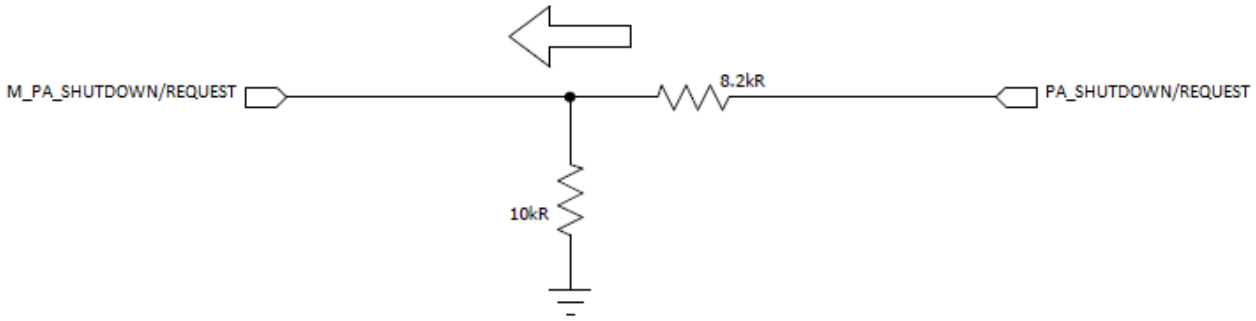


Figure 13. Zigbee_RNR

11 References

1. WL18xxMOD product page: http://www.ti.com/lsds/ti/wireless_connectivity/wilink/products.page
2. Texas Instruments: *Level Shifting WL18xx I/Os Application Report*
3. *WL18xx Adding WoWLAN* wiki: http://processors.wiki.ti.com/index.php/WL18xx_Adding_WoWLAN
4. Texas Instruments: *WL1837MODCOM8I WLAN MIMO and Bluetooth® Module Evaluation Board for TI Sitara™ Platform User's Guide*

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (August 2018) to B Revision	Page
• Update was made in the Asbstract of this document.	1

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