

MOSFET - Power, Single N-Channel, PQFN8 5x6 150 V, 11.5 mΩ, 78 A



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NTMFS011N15MC

Features

- Small Footprint (5 x 6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Synchronous Rectification
- AC-DC and DC-DC Power Supplies
- AC-DC Adapters (USB PD) SR
- Load Switch

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$, Unless otherwise specified)

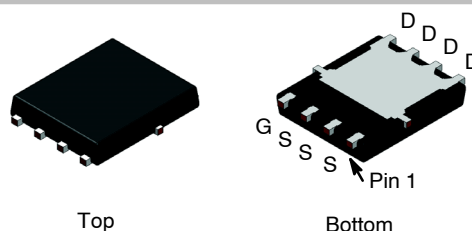
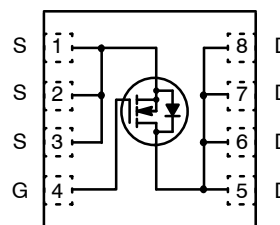
Parameter			Symbol	Value	Unit
Drain-to-Source Breakdown Voltage			$V_{(BR)DSS}$	150	V
Gate-to-Source Voltage			V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	$T_C = 25^\circ\text{C}$	I_D	78	A
			P_D	147	W
Continuous Drain Current $R_{\theta JA}$ (Note 1, 2)	Steady State	$T_A = 25^\circ\text{C}$	I_D	10.7	A
			P_D	2.7	W
Pulsed Drain Current	$T_A = 25^\circ\text{C}$, $t_p = 250 \mu\text{s}$	I_{DM}	259	A	
Operating Junction and Storage Temperature			T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Source Current (Body Diode)			I_S	133	A
Single Pulse Drain-to-Source Avalanche Energy ($I_{AV} = 39 \text{ A}$, $L = 0.1 \text{ mH}$)			E_{AS}	76.1	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)			T_L	300	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using 1 in² pad size, 1 oz Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
150 V	11.5 mΩ @ 10 V	35 A
	13.2 mΩ @ 8 V	18 A

N-Channel MOSFET

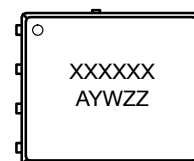


Top

Bottom

PQFN8 5x6
(Power 56)
CASE 483AE

MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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THERMAL CHARACTERISTICS

Symbol	Parameter	Max	Unit
$R_{\theta JC}$	Junction-to-Case – Steady State (Note 5)	0.85	°C/W
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Note 5)	46	

ORDERING INFORMATION

Device	Device Marking	Package	Shipping (Qty / Packing) [†]
NTMFS011N15MC	NTMFS011N15MC	PQFN8 5x6 (Power 56) (Pb-Free/Halogen Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

$V_{(BR)DSS}$	Drain – to – Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	150			V
$V_{(BR)DSS} / T_J$	Drain – to – Source Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}, \text{ref to } 25^\circ\text{C}$		85		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{GS} = 0\text{ V}, V_{DS} = 120\text{ V}$	$T_J = 25^\circ\text{C}$		1	μA
			$T_J = 125^\circ\text{C}$		100	
I_{GSS}	Gate – to – Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 3)

$V_{GS(TH)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 194\ \mu\text{A}$	2.5	3.35	4.5	V
$V_{GS(TH)} / I_J$	Negative Threshold Temperature Coefficient	$I_D = 250\ \mu\text{A}, \text{ref to } 25^\circ\text{C}$		-7.2		mV/°C
$R_{DS(on)}$	Drain – to – Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 35\text{ A}$		9.0	11.5	m Ω
		$V_{GS} = 8\text{ V}, I_D = 18\text{ A}$		9.7	13.2	
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 18\text{ A}$		96	116	S
R_G	Gate-Resistance	$T_A = 25^\circ\text{C}$		0.9	1.1	Ω

CHARGES & CAPACITANCES

C_{ISS}	Input Capacitance	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 75\text{ V}$		2478	3592	pF
C_{OSS}	Output Capacitance			728	1092	
C_{RSS}	Reverse Transfer Capacitance			7.9	15	
$Q_{G(TOT)}$	Total Gate Charge	$V_{GS} = 8\text{ V}, V_{DS} = 75\text{ V}, I_D = 35\text{ A}$		30.6	46	nC
$Q_{G(TOT)}$	Total Gate Charge	$V_{GS} = 10\text{ V}, V_{DS} = 75\text{ V}, I_D = 35\text{ A}$		30.7	46	
Q_{GS}	Gate-to-Source Charge			12.8		
Q_{SW}	Switching Charge			9.4		
Q_{GD}	Gate-to-Drain Charge			4.5		
Q_{OSS}	Output Charge	$V_{GS} = 0\text{ V}, V_{DD} = 75\text{ V}$		95		
V_{GP}	Plateau Voltage	$V_{GS} = 10\text{ V}, V_{DS} = 75\text{ V}, I_D = 35\text{ A}$		5.1		

SWITCHING CHARACTERISTICS (Note 3)

$t_{d(ON)}$	Turn – On Delay Time	$V_{GS} = 10\text{ V}, V_{DS} = 75\text{ V}, I_D = 35\text{ A}, R_G = 6\ \Omega$		19.8		ns
t_r	Rise Time			4.7		
$t_{d(OFF)}$	Turn – Off Delay Time			25.5		
t_f	Fall Time			4.0		

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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DRAIN-SOURCE DIODE CHARACTERISTICS

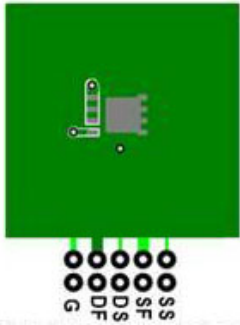
V_{SD}	Forward Diode Voltage	$V_{GS} = 0\text{ V}, I_S = 35\text{ A}$	$T_J = 25^\circ\text{C}$	0.869		V
			$T_J = 125^\circ\text{C}$	0.725		
t_{RR}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, dI_S/dt = 300\text{ A}/\mu\text{s}, I_S = 35\text{ A}$		48.8		ns
Q_{RR}	Reverse Recovery Charge			227		nC
t_{RR}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, dI_S/dt = 1000\text{ A}/\mu\text{s}, I_S = 35\text{ A}$		36.4		ns
Q_{RR}	Reverse Recovery Charge			407		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

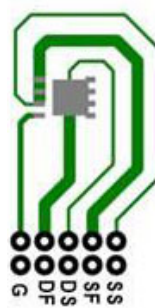
3. Switching characteristics are independent of operating junction temperatures.

NOTES:

4. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta CA}$ is determined by the user's board design.



a) 46°C/W when mounted on a 1 in² pad of 2 oz copper.



b) 116°C/W when mounted on a minimum pad of 2 oz copper.

5. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

6. E_{AS} of 196 mJ is based on starting $T_J = 25^\circ\text{C}$; $L = 3\text{ mH}$, $I_{AS} = 12.7\text{ A}$, $V_{DD} = 100\text{ V}$, $V_{GS} = 15\text{ V}$. 100% tested at $L = 0.1\text{ mH}$, $I_{AS} = 41\text{ A}$.

7. Pulsed I_D please refer to Fig 11 SOA graph for more details.

8. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

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TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted.)

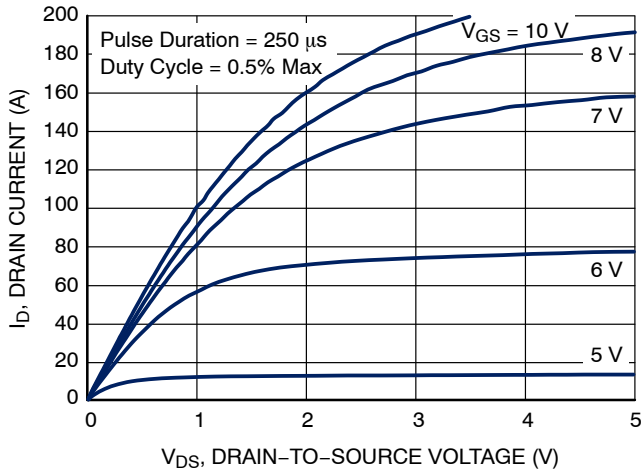


Figure 1. On-Region Characteristics

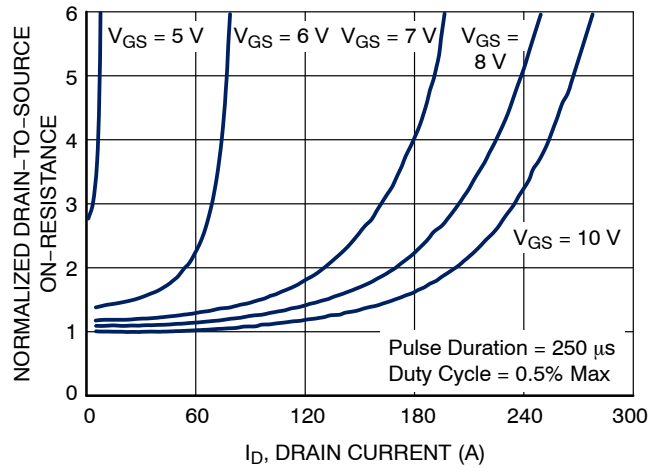


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

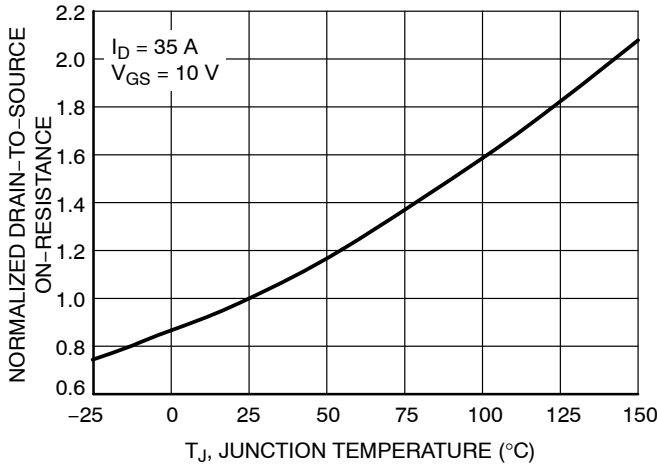


Figure 3. Normalized On-Resistance vs. Junction Temperature

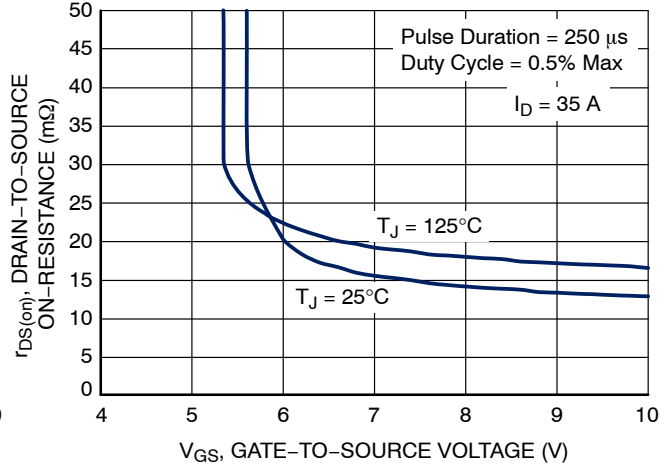


Figure 4. On-Resistance vs. Gate-to-Source Voltage

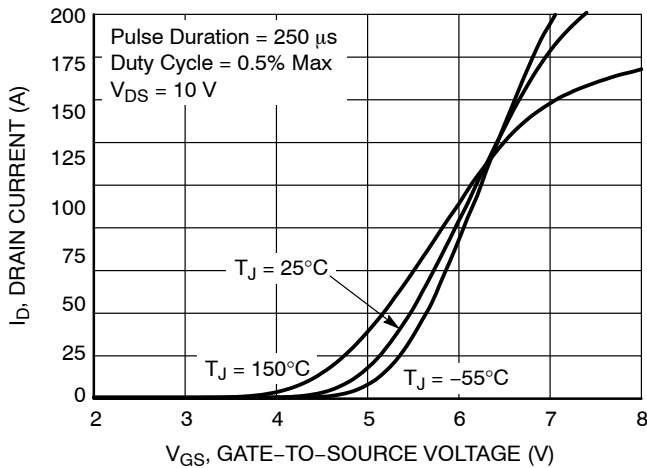


Figure 5. Transfer Characteristics

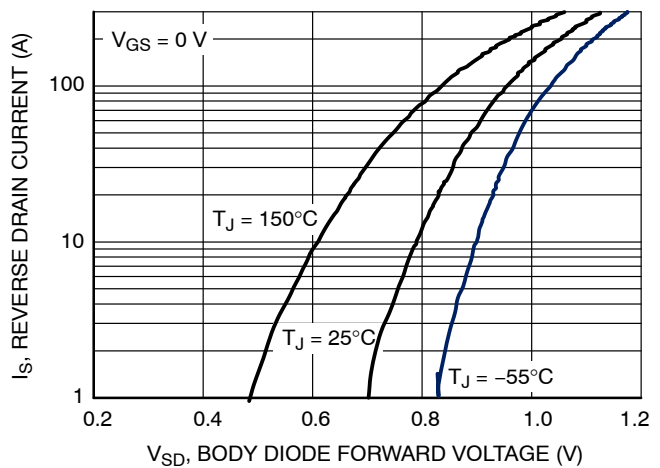


Figure 6. Source-to-Drain Diode Forward Voltage vs. Source Current

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TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted.)

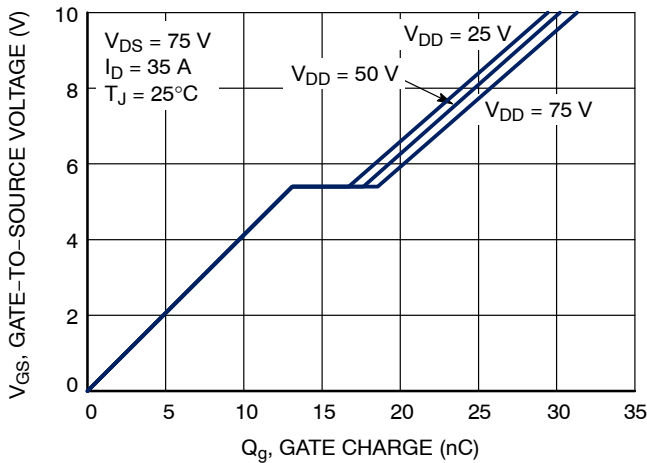


Figure 7. Gate Charge Characteristics

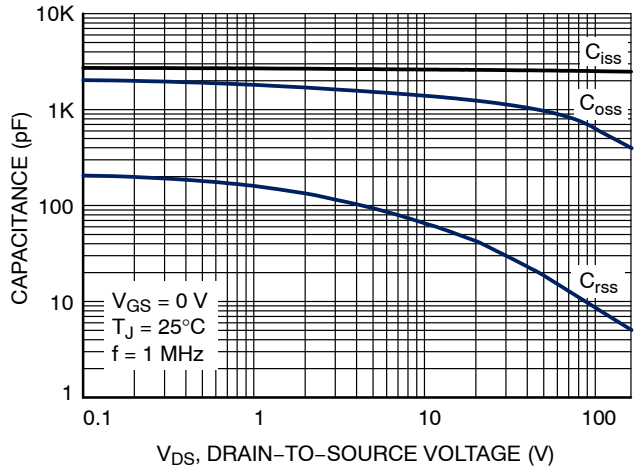


Figure 8. Capacitance vs. Drain-to-Source Voltage

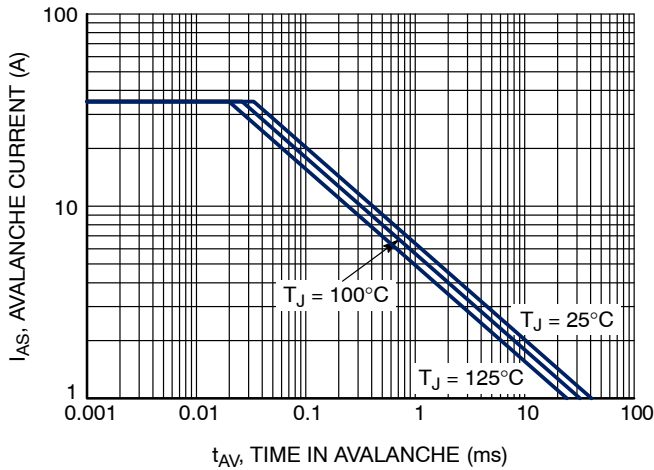


Figure 9. Unclamped Inductive Switching Capability

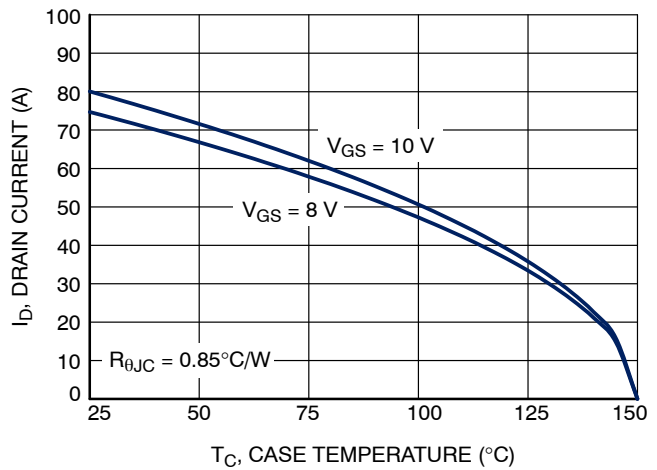


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

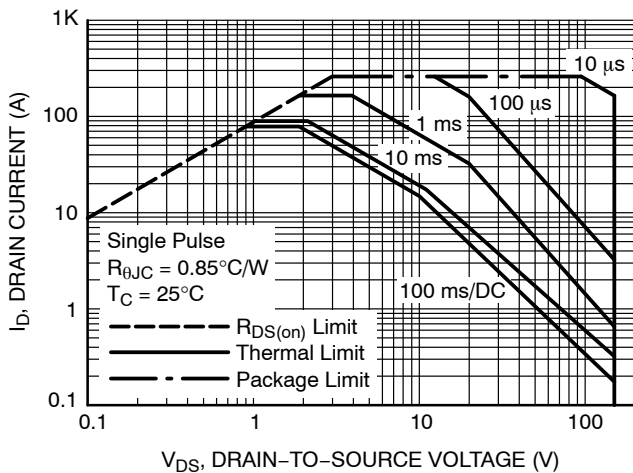


Figure 11. Forward Bias Safe Operating Area

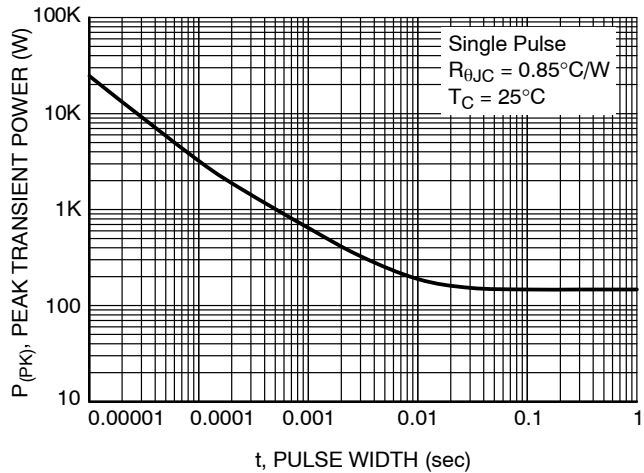


Figure 12. Single Pulse Maximum Power Dissipation

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TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted.)

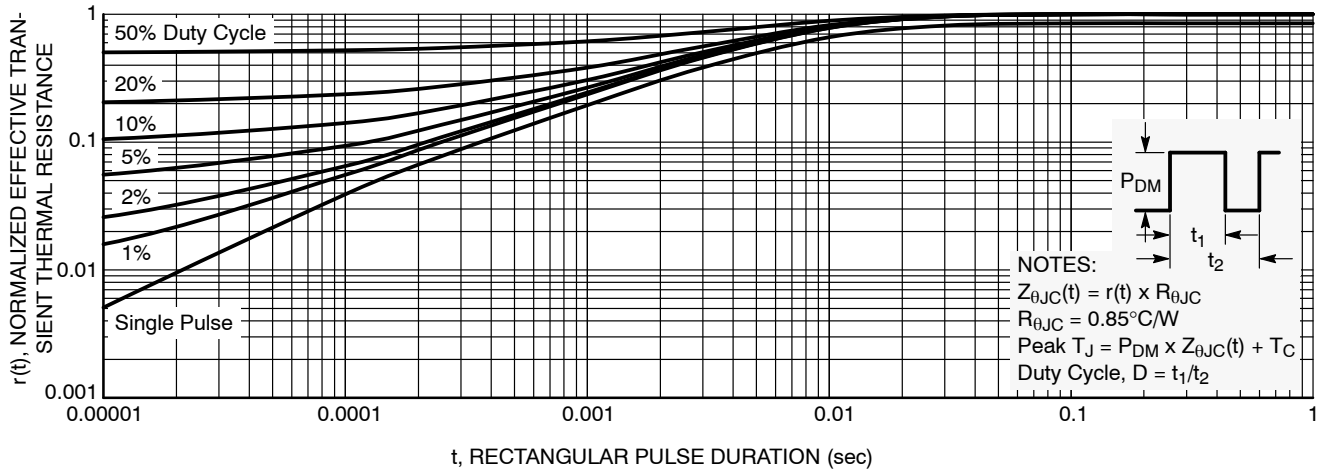


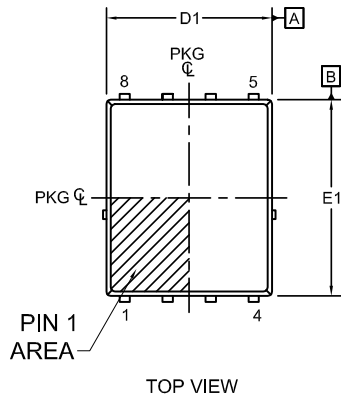
Figure 13. Junction-to-Case Transient Thermal Response Curve

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



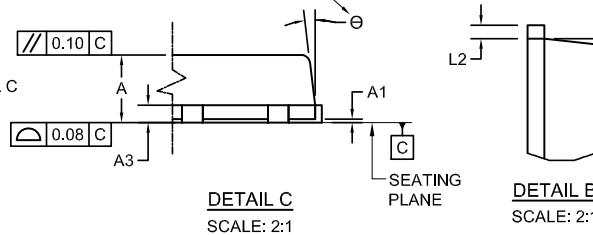
PQFN8 5X6, 1.27P
CASE 483AE
ISSUE C

DATE 21 JAN 2022

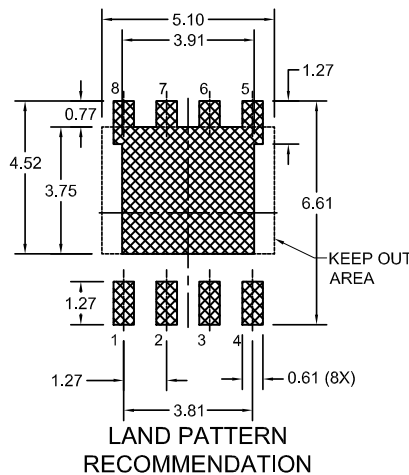
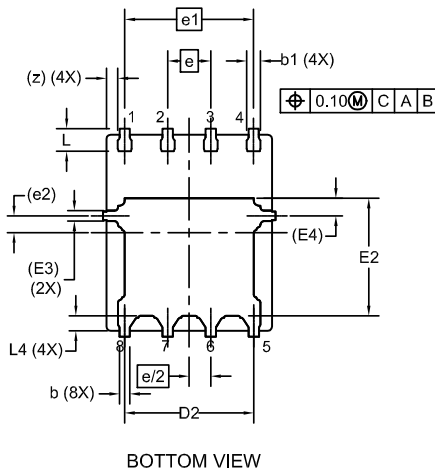


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.21	0.31	0.41
b1	0.31	0.41	0.51
A3	0.15	0.25	0.35
D	4.90	5.00	5.20
D1	4.80	4.90	5.00
D2	3.61	3.82	3.96
E	5.90	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.78
E3	0.30 REF		
E4	0.52 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
e2	0.50 REF		
L	0.51	0.66	0.76
L2	0.05	0.18	0.30
L4	0.34	0.44	0.54
z	0.34 REF		
θ	0°	-	12°



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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