CHANGE NOTIFICATION

Analog Devices, Inc.
1630 McCarthy Blvd., Milpitas CA
(408) 432-1900

December 7, 2017 PCN_120717

Dear Sir/Madam:

Subject: Notification of Change to LTC3546

Please be advised that Analog Devices, Inc. Milpitas, California has made a minor change to the LTC3546 product datasheet to facilitate improvement in our manufacturing capability. The changes are shown on the attached pages of the mark-up datasheet. There was no change in form, fit, function, quality or reliability of the product. The product shipped after February 7, 2018 will be tested to the new limits.

Should you have any questions or concerns please contact your local Analog Devices sales representatives or you may contact me at 408-432-1900 ext. 2077, or by e-mail at JASON.HU@ANALOG.COM. If I do not hear from you by February 7, 2018, we will consider this change to be approved by your company.

Sincerely,

Jason Hu
Quality Assurance Engineer

For questions on this PCN, please contact Jason Hu or you may send an email to your regional contacts below or contact your local ADI sales representatives.			
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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{CCA} = 3.6V, unless otherwise specified. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN1}, V_{IN1D}, V_{IN2}, V_{CCA}, V_{CCD}	Operating Voltage Range	V_{IN1} = V_{IN1D} = V_{IN2} = V_{CCA} = V_{CCD}		2.25 → 2.3		5.5	V
I_{FB1}, I_{FB2}	Feedback Pin Input Current	(Note 3)				±0.1	µA
V_{FB1}, V_{FB2}	Feedback Voltage	(Note 3) 2.3V	●	0.588	0.6	0.612	V
$\Delta V_{LINEREG}$	Reference Voltage Line Regulation %/V is The Percentage Change in V_{OUT} with a Change in V_{IN}	V_{IN} = 2.25V to 5.5V (Note 3)			0.04	0.2	%/V
$\Delta V_{LOADREG}$	Output Voltage Load Regulation	I_{TH1}, I_{TH2} = 0.36V (Note 3) I_{TH1}, I_{TH2} = 0.84V (Note 3)	● ●		0.02 –0.02	0.2 –0.2	% %
$g_{m(EA)}$	Error Amplifier Transconductance	(Note 3)			1400		µS
$V_{TRACK/SS1}$, $V_{TRACK/SS2}$	Tracking Voltage Offset	$V_{TRACK/SS1,2}$ = 0.3V				15	mV
$I_{TRACK/SS1}$, $I_{TRACK/SS2}$	Tracking Current Source	$V_{TRACK/SS1,2}$ = 0V		0.8	1.15	1.5	µA
I_S	Input DC Supply Current (Note 4)						
	Active Mode	V_{FB1} = V_{FB2} = 0.55V, V_{MODE} = V_{IN}, V_{RUN1} = V_{RUN2} = V_{IN}			600	990	µA
	Half Active Mode (V_{RUN1} = V_{IN}, V_{RUN2} = 0)	V_{FB1} = 0.55V, V_{MODE} = V_{IN}, V_{RUN1} = V_{IN}, V_{RUN2} = 0V			400	800	µA
	Half Active Mode (V_{RUN1} = 0, V_{RUN2} = V_{IN})	V_{FB2} = 0.55V, V_{MODE} = V_{IN}, V_{RUN1} = 0V, V_{RUN2} = V_{IN}			400	800	µA
	Both Channels in Sleep Mode	V_{FB1} = V_{FB2} = 0.75V, V_{MODE} = V_{IN}, V_{RUN1} = V_{RUN2} = V_{IN}			160	300	µA
	Shutdown	V_{RUN1} = V_{RUN2} = 0V			0.2	1	µA
f_{OSC}	Oscillator Frequency	V_{FREQ}: R_T = V_{IN} V_{FREQ}: R_T = 143k V_{FREQ}: Resistor (Note 5)	 ● 	1.8 1.2 0.75	2.25 1.5	2.9 1.8 4	MHz MHz MHz
I_{LIM1}	Peak Switch Current Limit on SW1 (1A)	BMC1 = V_{IN}, V_{ITH1} = 1.4V BMC1 = 0.4V, V_{ITH1} = 0V		1.4	1.6 0.45		A A
I_{LIM2}	Peak Switch Current Limit on SW2A/B (2A)	BMC2 = V_{IN}, V_{ITH1} = 1.4V BMC2 = 0.4V, V_{ITH1} = 0V		2.8	3.2 0.9		A A
$I_{LIM1+1D}$	Peak Switch Current Limit on SW1 + SW1D (2A)	SW1 Externally Connected to SW1D BMC1 = V_{IN} (Note 8) BMC1 = 0.4V (Note 8)		 2.5	 3.2 1.6		 A A
$I_{LIM2+1D}$	Peak Switch Current Limit on SW2A/B + SW1D (3A)	SW2A/B Externally Connected to SW1D BMC2 = V_{IN} (Note 8) BMC2 = 0.4V (Note 8)		 3.75	 4.8 2.4		 A A
$R_{DS(ON)1}$	SW1 Top Switch On-Resistance (1A) SW1 Bottom Switch On-Resistance	V_{IN2} = 3.6V V_{IN2} = 3.6V			0.19 0.18		Ω Ω
$R_{DS(ON)1D}$	SW1D Top Switch On-Resistance (1A) SW1D Bottom Switch On-Resistance	V_{IN2} = 3.6V V_{IN2} = 3.6V			0.19 0.17		Ω Ω
$R_{DS(ON)2}$	SW2A/B Top Switch On-Resistance (2A) SW2A/B Bottom Switch On-Resistance	V_{IN1} = 3.6V V_{IN1} = 3.6V			0.096 0.085		Ω Ω
$I_{SW1(LKG)}$	Switch Leakage Current SW1	V_{IN} = 6V V_{ITH1} = 0V V_{RUN1} = 0V			0.01	1	µA

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{SW1D(LKG)}$	Switch Leakage Current SW1D	V_{IN} = 6V V_{ITH1} = V_{ITH2} = 0V V_{RUN1} = V_{RUN2} = 0V			0.01	1	µA
$I_{SW2A/B(LKG)}$	Switch Leakage Current SW2A/B	V_{IN} = 6V V_{ITH2} = 0V V_{RUN2} = 0V			0.01	1	µA
V_{UVLO}	Undervoltage Lockout Threshold	V_{IN1}, V_{IN2}, V_{CCA}, V_{CCD} Rising V_{IN1}, V_{IN2}, V_{CCA}, V_{CCD} Falling		2.03 1.86	2.14 1.97	~~2.2~~ 2.28 ~~2.03~~ 2.11	V V
T_{PGOOD1}	Threshold for Power Good Percentage Deviation from Regulated V_{FB1} (Typically 0.6V).	V_{FB1} Ramping Up, $V_{SYNC/MODE}$ = 0V			–8		%
T_{PGOOD2}	Threshold for Power Good Percentage Deviation from Regulated V_{FB2} (Typically 0.6V).	V_{FB2} Ramping Up, $V_{SYNC/MODE}$ = 0V			–8		%
R_{PGOOD1}	Power Good Pull-Down On-Resistance				132	300	Ω
R_{PGOOD2}	Power Good Pull-Down On-Resistance				132	300	Ω
t_{SS}	Soft-Start Internal Time.	V_{FB} from 0% to 95%, $V_{TRACK/SS}$ Is Floating		0.8	1.2	1.9	ms
V_{RUN1}, V_{RUN2}, V_{PHASE}	RUN1, RUN2, and PHASE Threshold			0.3	0.8	1.2	V
I_{RUN1}, I_{RUN2}, I_{PHASE}	RUN1, RUN2, and PHASE Leakage Current	V_{IN} = 6V, V_{PHASE} = 3V, V_{RUN1} = V_{RUN2} = 3V			±0.01	±1	µA
$VTL_{SYNC/MODE}$	SYNC/MODE Threshold Voltage Low to Put the Part into Pulse-Skipping Mode					0.5	V
$VTH_{SYNC/MODE}$	SYNC/MODE Threshold Voltage High to Put the Part into Burst Mode Operation			V_{IN} – 0.5			V
$V_{SYNC/MODE}$	SYNC/MODE Threshold for Clock Synchronization			0.3	0.8	1.2	V
$I_{SYNC/MODE}$	SYNC/MODE Leakage Current	V_{IN} = 6V, $V_{SYNC/MODE}$ = 3V			±0.01	±1	µA
VTH_{FREQ}	FREQ Threshold Voltage High			V_{IN} – 0.85			V
I_{BMC1}, I_{BMC2}	BMC1, BMC2 Leakage Current	V_{IN} = 6V, V_{BMC} = 3V				±0.4	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3546 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3546E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3546I is guaranteed to meet performance specifications over the full –40°C to 125°C operating junction temperature range. The maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: The LTC3546 is tested in feedback loop which servos V_{FB1} to the midpoint for the error amplifier (V_{ITH1} = 0.6V) and V_{FB2} to the midpoint for the error amplifier (V_{ITH2} = 0.6V).

Note 4: Total supply current is higher due to the internal gate charge being delivered at the switching frequency.

Note 5: Variable frequency operation with resistor is guaranteed by design and is subject to duty cycle limitations.

Note 6: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 7: T_J is calculated from the ambient temperature, T_A, and power dissipation, P_D, according to the following formula:

$T_J = T_A + (P_D \bullet 34°C/W)$

Note 8: Minimum current limit is guaranteed by design and correlation to the $R_{DS(ON)1D}$, I_{LIM1} and I_{LIM2} measurements.