

# HEF4543B

## BCD to 7-segment latch/decoder/driver

Rev. 7 — 1 April 2016

Product data sheet

### 1. General description

The HEF4543B is a BCD to 7-segment latch/decoder/driver for liquid crystal and LED displays. It has four address inputs (D0 to D3), an active LOW latch enable input ( $\overline{LE}$ ), an active HIGH blanking input (BL), an active HIGH phase input (PH) and seven buffered segment outputs (Qa to Qg).

The circuit provides the function of a 4-bit storage latch and an 8-4-2-1 BCD to 7-segment decoder/driver. It can invert the logic levels of the output combination. The phase (PH), blanking (BL) and latch enable ( $\overline{LE}$ ) inputs are used to reverse the function table phase, blank the display and store a BCD code, respectively.

For liquid crystal displays, a square-wave is applied to PH and the electrical common back-plane of the display. The outputs of the device are directly connected to the segments of the liquid crystal.

It operates over a recommended  $V_{DD}$  power supply range of 3 V to 15 V referenced to  $V_{SS}$  (usually ground). Unused inputs must be connected to  $V_{DD}$ ,  $V_{SS}$ , or another input.

### 2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B

### 3. Ordering information

Table 1. Ordering information

All types operate from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$

Type number	Package		Version
	Name	Description	
HEF4543BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

4. Functional diagram

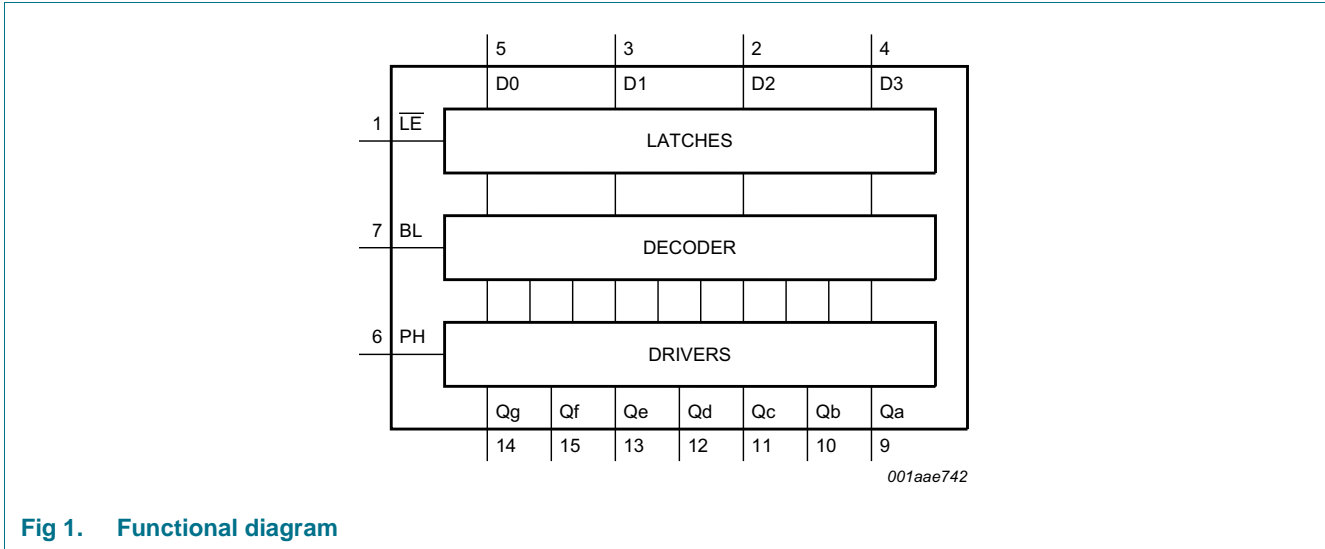


Fig 1. Functional diagram

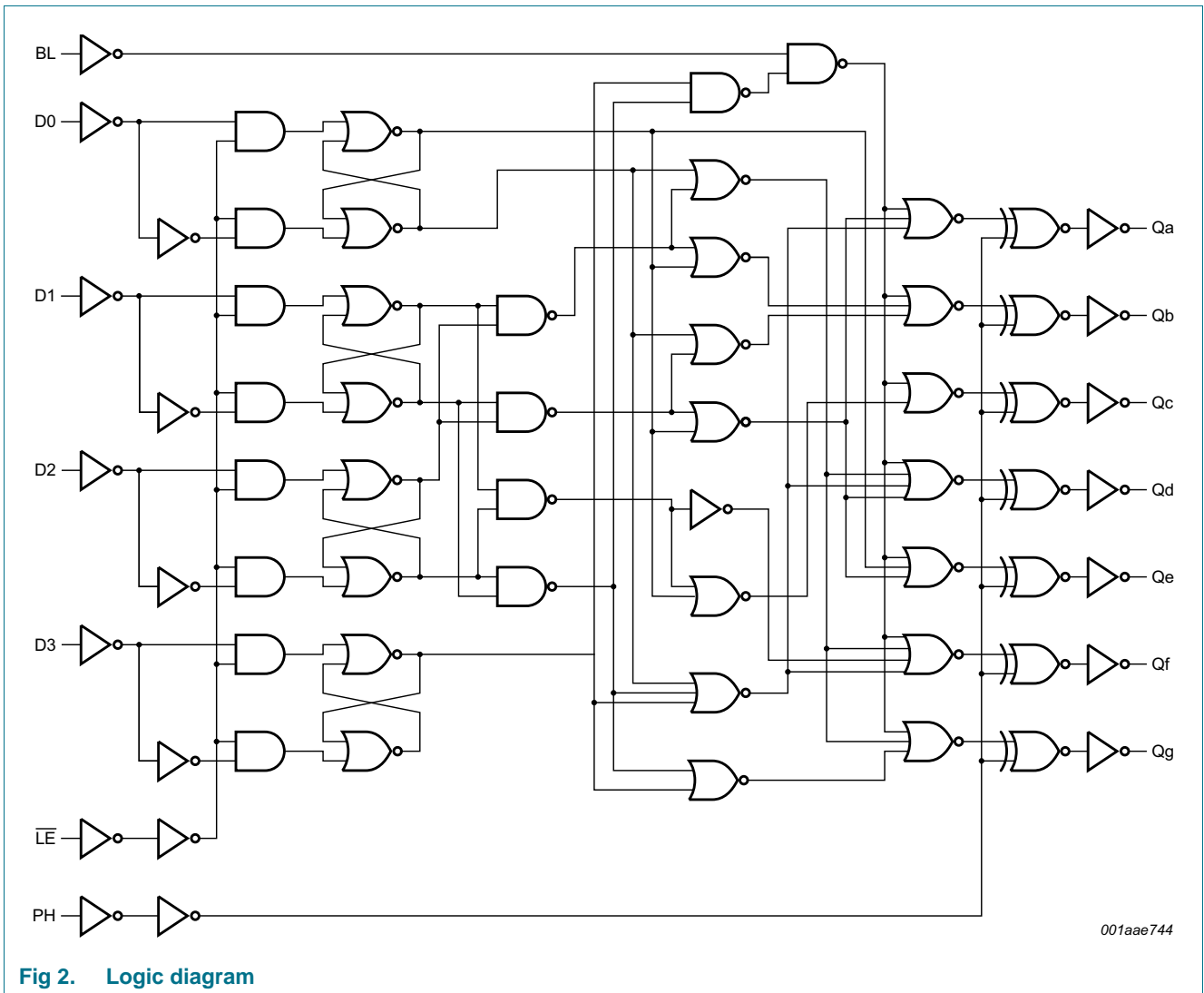


Fig 2. Logic diagram

## 5. Pinning information

### 5.1 Pinning

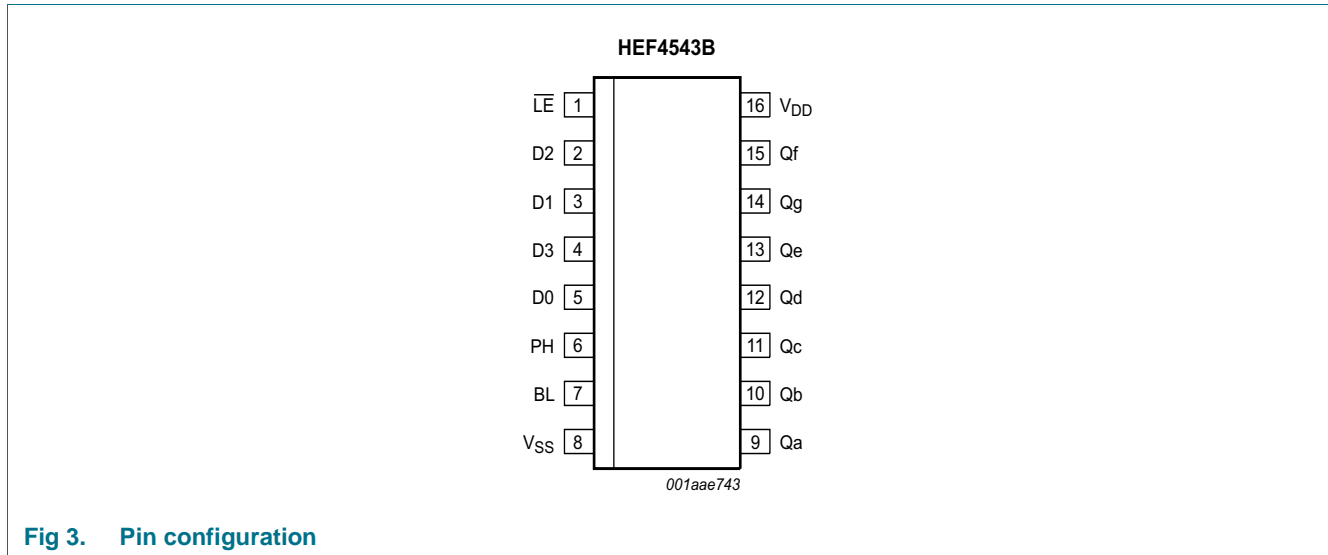


Fig 3. Pin configuration

### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{\text{LE}}$	1	latch enable input (active LOW)
D0 to D3	5, 3, 2, 4	address (data) input
PH	6	phase input (active HIGH)
BL	7	blanking input (active HIGH)
$V_{\text{SS}}$	8	ground supply voltage
Qa to Qg	9, 10, 11, 12, 13, 15, 14	segment output
$V_{\text{DD}}$	16	supply voltage

## 6. Functional description

Table 3. Function table [1]

Inputs							Outputs							Display
LE	BL	PH [2]	D3	D2	D1	D0	Qa	Qb	Qc	Qd	Qe	Qf	Qg	
X	H	L	X	X	X	X	L	L	L	L	L	L	L	blank
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	L	H	X	L	L	L	L	L	L	L	blank
H	L	L	H	H	X	X	L	L	L	L	L	L	L	blank
L	L	L	X	X	X	X	n.c.							n.c.
as above		H	as above				inverse of above							as above

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; n.c. = no change.

[2] For liquid crystal displays, apply a square-wave to PH;  
 For common cathode LED displays, select PH = LOW;  
 For common anode LED displays, select PH = HIGH.

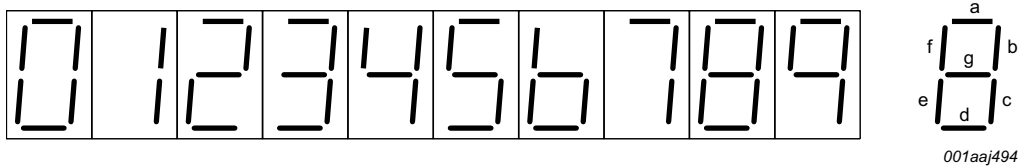


Fig 4. Seven segment digital display with segment designation

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		-0.5	+18	V
$V_I$	input voltage		-0.5	$V_{DD} + 0.5$	V
$I_{I/O}$	input/output current		-	$\pm 10$	mA
$T_{stg}$	storage temperature		-65	+150	°C

**Table 4.** Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{amb}$	ambient temperature		-40	+85	°C
$P_{tot}$	total power dissipation	SO16 package [1]	-	500	mW
$P$	power dissipation	per output	-	100	mW

[1] For SO16 package:  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.

## 8. Recommended operating conditions

**Table 5.** Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD}$	supply voltage		3	-	15	V
$V_I$	input voltage		0	-	$V_{DD}$	V
$T_{amb}$	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	-	3.75	μs/V
		$V_{DD} = 10\text{ V}$	-	-	0.5	μs/V
		$V_{DD} = 15\text{ V}$	-	-	0.08	μs/V

## 9. Static characteristics

**Table 6.** Static characteristics $V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	$T_{amb} = -40\text{ °C}$		$T_{amb} = 25\text{ °C}$		$T_{amb} = 85\text{ °C}$		Unit
				Min	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
$V_{IL}$	LOW-level input voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
$V_{OH}$	HIGH-level output voltage		5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
$V_{OL}$	LOW-level output voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
$I_{OH}$	HIGH-level output current	$V_O = 2.5\text{ V}$	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		$V_O = 4.6\text{ V}$	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		$V_O = 9.5\text{ V}$	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		$V_O = 13.5\text{ V}$	15 V	-	-3.6	-	-3.0	-	-2.4	mA

**Table 6. Static characteristics ...continued**  
 $V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	$T_{amb} = -40\text{ °C}$		$T_{amb} = 25\text{ °C}$		$T_{amb} = 85\text{ °C}$		Unit
				Min	Max	Min	Max	Min	Max	
$I_{OL}$	LOW-level output current	$V_O = 0.4\text{ V}$	5 V	0.52	-	0.44	-	0.36	-	mA
		$V_O = 0.5\text{ V}$	10 V	1.3	-	1.1	-	0.9	-	mA
		$V_O = 1.5\text{ V}$	15 V	3.6	-	3.0	-	2.4	-	mA
$I_I$	input leakage current		15 V	-	$\pm 0.3$	-	$\pm 0.3$	-	$\pm 1.0$	$\mu\text{A}$
$I_{DD}$	supply current	$I_O = 0\text{ A}$	5 V	-	20	-	20	-	150	$\mu\text{A}$
			10 V	-	40	-	40	-	300	$\mu\text{A}$
			15 V	-	80	-	80	-	600	$\mu\text{A}$
$C_I$	input capacitance		-	-	-	7.5	-	-	pF	

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**  
 $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ; For test circuit see [Figure 7](#); unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	Extrapolation formula <sup>[1]</sup>	Min	Typ	Max	Unit
$t_{PHL}$	HIGH to LOW propagation delay	Dn to Qn; see <a href="#">Figure 5</a>	5 V	$153\text{ ns} + (0.55\text{ ns/pF})C_L$	-	180	360	ns
			10 V	$64\text{ ns} + (0.23\text{ ns/pF})C_L$	-	75	150	ns
			15 V	$47\text{ ns} + (0.16\text{ ns/pF})C_L$	-	55	110	ns
		$\overline{LE}$ to Qn; see <a href="#">Figure 5</a>	5 V	$143\text{ ns} + (0.55\text{ ns/pF})C_L$	-	170	340	ns
			10 V	$69\text{ ns} + (0.23\text{ ns/pF})C_L$	-	80	160	ns
			15 V	$52\text{ ns} + (0.16\text{ ns/pF})C_L$	-	60	120	ns
		BL to Qn; see <a href="#">Figure 5</a>	5 V	$118\text{ ns} + (0.55\text{ ns/pF})C_L$	-	145	290	ns
			10 V	$54\text{ ns} + (0.23\text{ ns/pF})C_L$	-	65	130	ns
			15 V	$37\text{ ns} + (0.16\text{ ns/pF})C_L$	-	45	90	ns
$t_{PLH}$	LOW to HIGH propagation delay	Dn to Qn; see <a href="#">Figure 5</a>	5 V	$153\text{ ns} + (0.55\text{ ns/pF})C_L$	-	180	360	ns
			10 V	$64\text{ ns} + (0.23\text{ ns/pF})C_L$	-	75	150	ns
			15 V	$47\text{ ns} + (0.16\text{ ns/pF})C_L$	-	55	110	ns
		$\overline{LE}$ to Qn; see <a href="#">Figure 5</a>	5 V	$163\text{ ns} + (0.55\text{ ns/pF})C_L$	-	190	380	ns
			10 V	$69\text{ ns} + (0.23\text{ ns/pF})C_L$	-	80	160	ns
			15 V	$52\text{ ns} + (0.16\text{ ns/pF})C_L$	-	60	120	ns
		BL to Qn; see <a href="#">Figure 5</a>	5 V	$98\text{ ns} + (0.55\text{ ns/pF})C_L$	-	125	250	ns
			10 V	$54\text{ ns} + (0.23\text{ ns/pF})C_L$	-	55	110	ns
			15 V	$32\text{ ns} + (0.16\text{ ns/pF})C_L$	-	40	80	ns
$t_t$	transition time	pin Qn; see <a href="#">Figure 5</a>	5 V	$10\text{ ns} + (1.00\text{ ns/pF})C_L$	-	60	120	ns
			10 V	$9\text{ ns} + (0.42\text{ ns/pF})C_L$	-	30	60	ns
			15 V	$6\text{ ns} + (0.28\text{ ns/pF})C_L$	-	20	40	ns
$t_{su}$	set-up time	Dn to $\overline{LE}$ ; see <a href="#">Figure 6</a>	5 V		40	20	-	ns
			10 V		20	5	-	ns
			15 V		15	0	-	ns

**Table 7. Dynamic characteristics ...continued**  
 $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ; For test circuit see [Figure 7](#); unless otherwise specified.

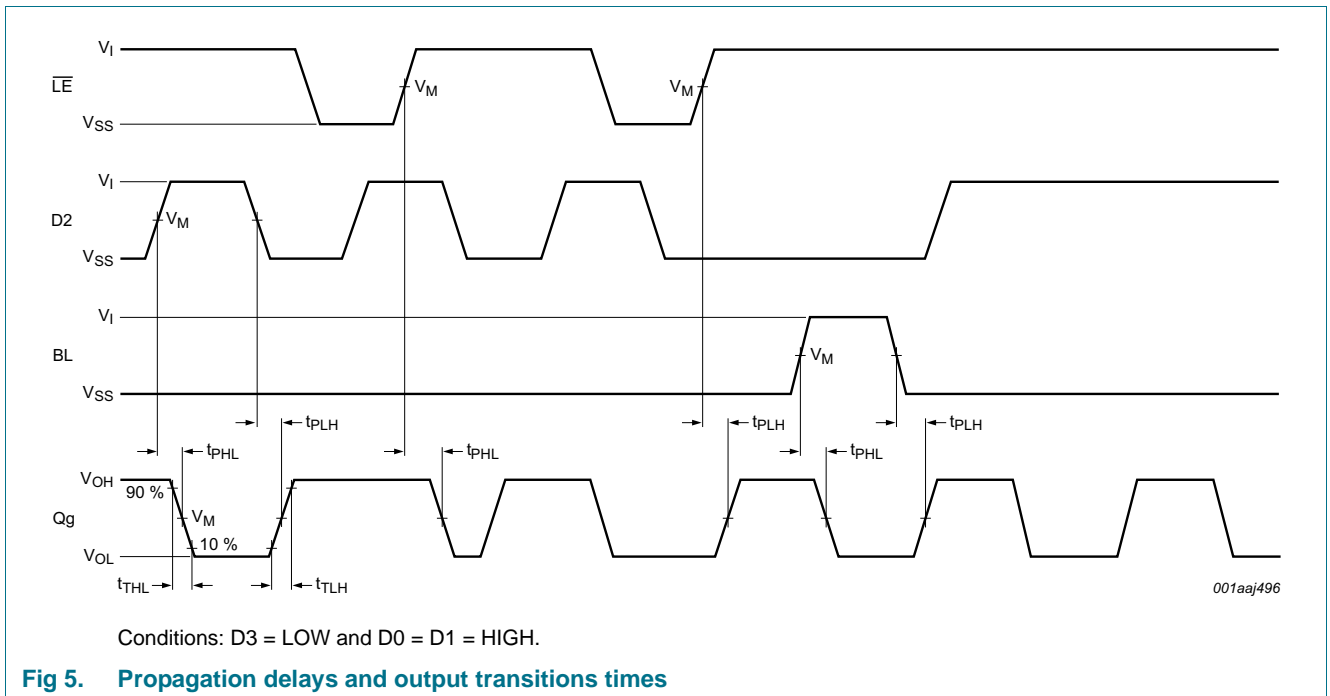
Symbol	Parameter	Conditions	$V_{DD}$	Extrapolation formula <sup>[1]</sup>	Min	Typ	Max	Unit
$t_h$	hold time	Dn to $\overline{LE}$ ; see <a href="#">Figure 6</a>	5 V		0	-15	-	ns
			10 V		15	0	-	ns
			15 V		20	5	-	ns
$t_w$	pulse width	pin $\overline{LE}$ HIGH; minimum width; see <a href="#">Figure 6</a>	5 V		60	30	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown ( $C_L$  in pF).

**Table 8. Dynamic power dissipation  $P_D$**   
 $P_D$  can be calculated from the formulas shown.  $V_{SS} = 0\text{ V}$ ;  $t_r = t_f \leq 20\text{ ns}$ ;  $T_{amb} = 25\text{ °C}$ .

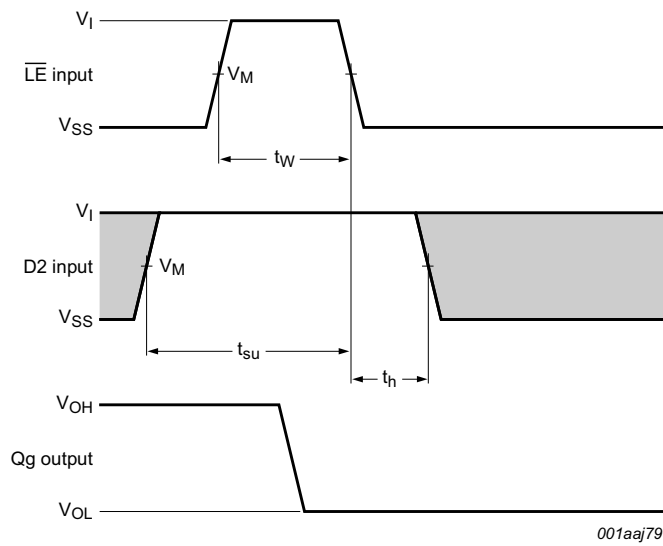
Symbol	Parameter	$V_{DD}$	Typical formula for $P_D$ ( $\mu\text{W}$ )	where:
$P_D$	dynamic power dissipation	5 V	$P_D = 2200 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$f_i$ = input frequency in MHz, $f_o$ = output frequency in MHz, $C_L$ = output load capacitance in pF, $V_{DD}$ = supply voltage in V, $\Sigma(C_L \times f_o)$ = sum of the outputs.
		10 V	$P_D = 10400 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	
		15 V	$P_D = 33000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	

## 11. Waveforms



**Fig 5. Propagation delays and output transitions times**



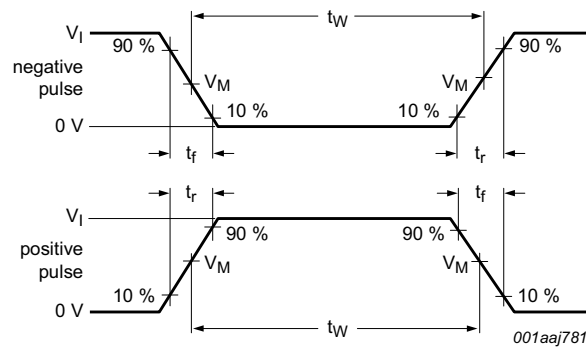


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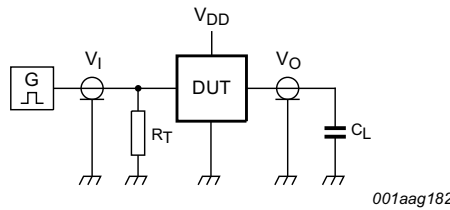
Conditions:

D3 = BL = LOW; D0 = D1 =  $\overline{LE}$  = HIGH

Fig 6. Waveforms showing minimum  $\overline{LE}$  pulse width, set-up, and hold time for DC to  $\overline{LE}$



a. Input waveforms



b. Test circuit

Test data is given in [Table 9](#).

Definitions for test circuit:

$R_L$  = Load resistance;

$C_L$  = Load capacitance including jig and probe capacitance;

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

Fig 7. Test circuit for measuring switching times

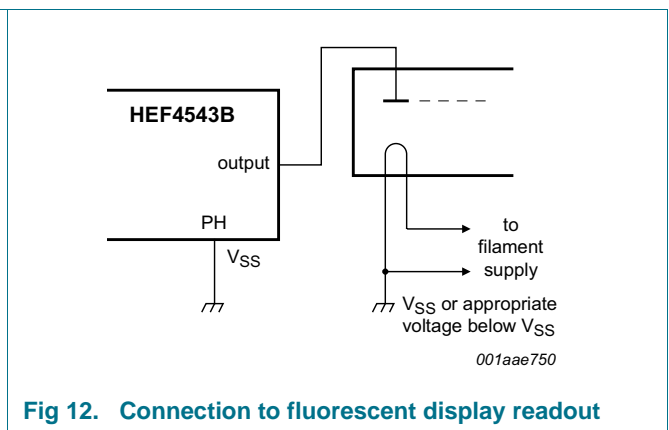
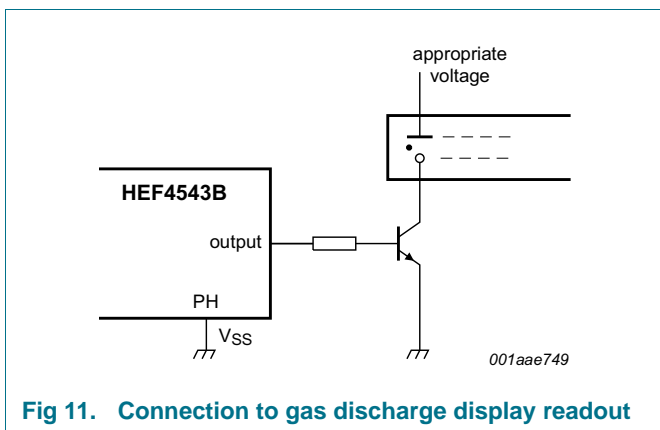
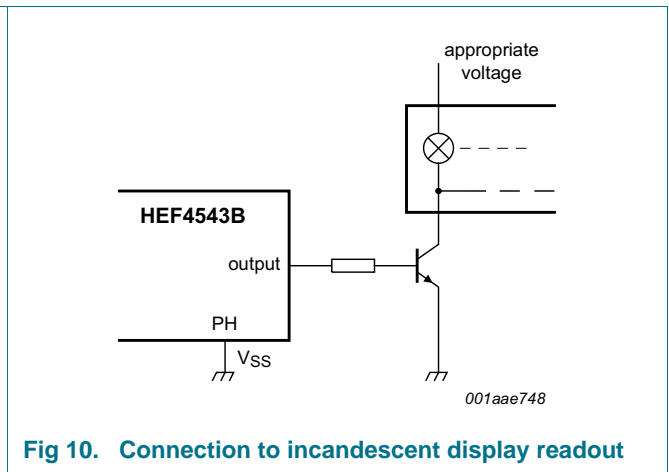
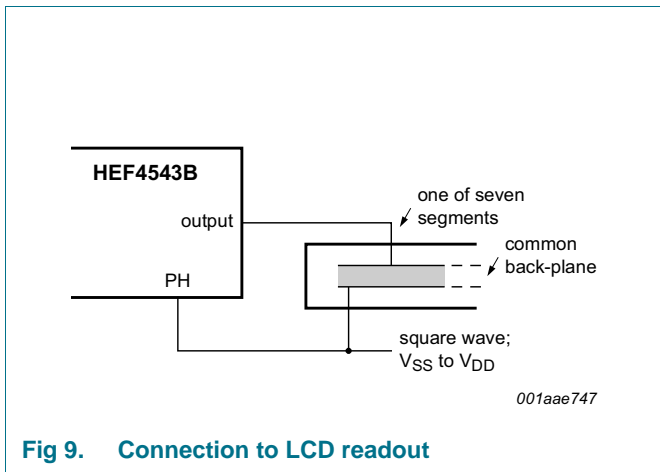
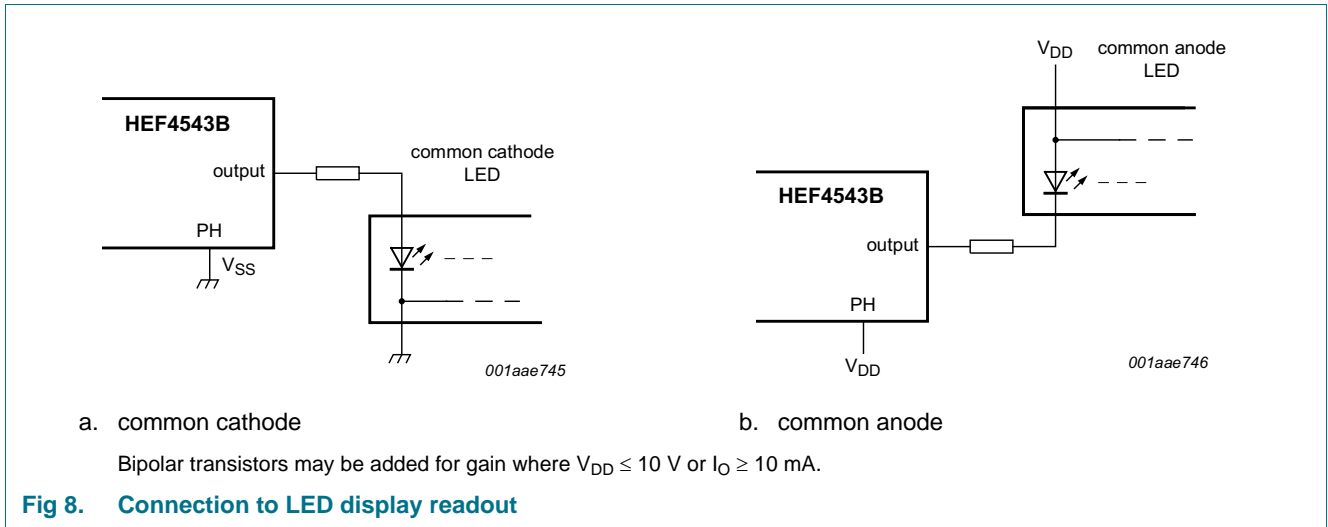
Table 9. Test data

Supply voltage	Input			Load
$V_{DD}$	$V_I$	$V_M$	$t_r, t_f$	$C_L$
5 V to 15 V	$V_{DD}$	$0.5V_I$	$\leq 20$ ns	50 pF

## 12. Application information

Some examples of applications for the HEF4543B are:

- Driving LCD displays
- Driving LED displays
- Driving fluorescent displays
- Driving incandescent displays
- Driving gas discharge displays



13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



Fig 13. Package outline SOT109-1 (SO16)

## 14. Abbreviations

Table 10. Abbreviations

Acronym	Description
DUT	Device Under Test

## 15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4543B v.7	20160401	Product data sheet	-	HEF4543B v.6
Modifications:	<ul style="list-style-type: none"> <li>Type number HEF4543BP (SOT38-4) removed.</li> </ul>			
HEF4543B v.6	20111117	Product data sheet	-	HEF4543B v.5
Modifications:	<ul style="list-style-type: none"> <li>Section Applications removed</li> <li><a href="#">Table 6</a>: I<sub>OH</sub> minimum values changed to maximum</li> <li><a href="#">Figure 6</a>: signal <math>\overline{LT}</math> removed; signal <math>\overline{BL}</math> replaced by BL (inverted)</li> </ul>			
HEF4543B v.5	20091027	Product data sheet	-	HEF4543B v.4
HEF4543B v.4	20090317	Product data sheet	-	HEF4543B_CNV v.3
HEF4543B_CNV v.3	19950101	Product specification	-	HEF4543B_CNV v.2
HEF4543B_CNV v.2	19950101	Product specification	-	-

## 16. Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

## 16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 17. Contact information

For more information, please visit: <http://www.nexperia.com>

For sales office addresses, please send an email to: [salesaddresses@nexperia.com](mailto:salesaddresses@nexperia.com)

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