CHANGE NOTIFICATION

Linear Technology Corporation
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November 12, 2013

Dear Sir/Madam: PCN# 111213

Subject: Notification of Change to LTC2978A Datasheet

Please be advised that Linear Technology Corporation has made a minor change to the LTC2978A Datasheet specification in order to improve device manufacturability. The changes are as mentioned below and shown on the attached page of the marked up datasheet.

ADC Characteristics
The ADC Characteristics were changed to specify only Total Unadjusted Error (TUE) rather than a combination of TUE, Gain Error, Offset, and INL. TUE is directly related to Gain Error, Offset, and INL by the following formula:

TUE (%) = Gain Error (%) + 100 * (INL + Offset) / Vin

The resulting, combined TUE spec is simpler and still provides the same information and the same performance guarantee in a system, while helping to improve yield and test time. In addition, the voltage condition at which TUE is specified was lowered from 1.8V to 1V. This guarantees an overall more accurate part:

1.8V * 0.25% = 4.5mV
1.0V * 0.25% = 2.5mV

Finally, this change makes all devices in the LTC Power System Manager family consistent by updating the LTC2978A and LTC2977 EC tables to match the LTC2974.

VOUT Enable, VIN Enable, and AUXFAULTB Output Characteristics
The Output High Voltage minimum was lowered to 10V. On certain process corners, the internal leakage currents were high enough to prevent the internal charge pump from reaching the minimum specified voltage. The minimum limit was lowered to accommodate these process corners. In most applications, these pins are externally pulled-up to 3.3V and this specification does not apply.

DAC Soft-Connect Comparator Offset
The EC table was clarified by adding test conditions to the original specification. Also, additional conditions were added to provide offset values more relevant to real applications. This specification only indicates the accuracy of the soft-connect algorithm, not the ability of the part to trim the output accurately. The effect of this offset on the output of the POL when the DAC connects is attenuated by the VDAC resistor and the feedback network. The trim accuracy is determined solely by the ADC accuracy.

The product die and the build sheet remain unchanged. A redlined datasheet characteristics table is attached. The product shipped after January 14th, 2014 will be tested to the new limits.

Should you have any further questions, please feel free to contact me at 408-432-1900 ext. 2077, or by email at JASON.HU@LINEAR.COM. If I do not hear from you by January 13th, 2014, we will consider this change to be approved by your company.

Sincerely,

Jason Hu
Quality Assurance Engineer

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. V_{PWR} = V_{IN_SNS} = 12V, V_{DD33}, V_{DD25}, REFP and REFM pins floating, unless otherwise indicated. C_{VDD33} = 100nF, C_{VDD25} = 100nF and C_{REF} = 100nF.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Characteristics							
V_{PWR}	V_{PWR} Supply Input Operating Range		●	4.5		15	V
I_{PWR}	V_{PWR} Supply Current	4.5V ≤ V_{PWR} ≤ 15V, V_{DD33} Floating	●		10	13	mA
I_{VDD33}	V_{DD33} Supply Current	3.13V ≤ V_{DD33} ≤ 3.47V, V_{PWR} = V_{DD33}	●		10	13	mA
V_{UVLO_VDD33}	V_{DD33} Undervoltage Lockout	V_{DD33} Ramping Up, V_{PWR} = V_{DD33}	●	2.35	2.55	2.8	V
	V_{DD33} Undervoltage Lockout Hysteresis				120		mV
V_{DD33}	Supply Input Operating Range	V_{PWR} = V_{DD33}	●	3.13		3.47	V
	Regulator Output Voltage	4.5V ≤ V_{PWR} ≤ 15V	●	3.13	3.26	3.47	V
	Regulator Output Short-Circuit Current	V_{PWR} = 4.5V, V_{DD33} = 0V	●	75	90	140	mA
V_{DD25}	Regulator Output Voltage	3.13V ≤ V_{DD33} ≤ 3.47V	●	2.35	2.5	2.6	V
	Regulator Output Short-Circuit Current	V_{PWR} = V_{DD33} = 3.47V, V_{DD25} = 0V	●	30	55	80	mA
t_{INIT}	Initialization Time	Time from V_{IN} Applied Until the TON_DELAY Timer Starts			135		ms
Voltage Reference Characteristics							
V_{REF}	Output Voltage	V_{REF} = V_{REFP} – V_{REFM}, 0 < I_{REFP} < 100µA			1.232		V
	Temperature Coefficient				3		ppm/°C
	Hysteresis	(Note 3)			100		ppm
ADC Characteristics							
V_{IN_ADC}	Voltage Sense Input Range	Differential Voltage: V_{IN_ADC} = ($V_{SENSEPn}$ – $V_{SENSEMn}$)	●	0		6	V
		Single-Ended Voltage: $V_{SENSEMn}$	●	–0.1		0.1	V
	Current Sense Input Range (Odd Numbered Channels Only)	Single-Ended Voltage: $V_{SENSEPn}$, $V_{SENSEMn}$	●	–0.1		6	V
		Differential Voltage: V_{IN_ADC}	●	–170		170	mV
N_ADC	Voltage Sense Resolution (Uses L16 Format)	0V ≤ V_{IN_ADC} ≤ 6V			122		µV/LSB
	Current Sense Resolution (Odd Numbered Channels Only)	0mV ≤ |V_{IN_ADC}| < 16mV (Note 11) 16mV ≤ |V_{IN_ADC}| < 32mV 32mV ≤ |V_{IN_ADC}| < 63.9mV 63.9mV ≤ |V_{IN_ADC}| < 127.9mV 127.9mV ≤ |V_{IN_ADC}|			15.625 31.25 62.5 125 250		µV/LSB µV/LSB µV/LSB µV/LSB µV/LSB
TUE_ADC_VOLT_SNS	Total Unadjusted Error	Voltage Sense Mode V_{IN_ADC} ≥ 1V	●			±0.25	% of Reading
		Voltage Sense Mode 0 ≤ V_{IN_ADC} ≤ 1V	●			±2.5	mV
TUE_ADC_CURR_SNS	Total Unadjusted Error	Current Sense Mode, Odd Numbered Channels Only; 20mV ≤ V_{IN_ADC} ≤ 170mV	●			±0.7	% of Reading
		Current Sense Mode, Odd Numbered Channels Only; V_{IN_ADC} ≤ 20mV	●			140	µV
V_{OS_ADC}	Offset Error	Current Sense Mode, Odd Numbered Channels Only	●			±35	µV
t_{CONV_ADC}	Conversion Time	Voltage Sense Mode (Note 4)			6.15		ms
		Current Sense Mode (Note 4)			24.6		ms
		Temperature Input (Note 4)			24.6		ms
t_{UPDATE_ADC}	Maximum Update Time	Odd Numbered Channels in Current Sense Mode (Note 4)			160		ms

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DAC Soft-Connect Comparator Characteristics							
V_{OS_CMP}	Offset Voltage	V_{DACPn} = 0.2V	●		±1	±18	mV
		V_{DACPn} = 1.3V	●		±2	±26	mV
		V_{DACPn} = 2.65V	●		±3	±52	mV
Temperature Sensor Characteristics							
TUE_TS	Total Unadjusted Error				±1		°C
V_{OUT} Enable Output (V_{OUT_EN} [3:0]) Characteristics							
V_{VOUT_ENn}	Output High Voltage (Note 10)	I_{VOUT_ENn} = –5µA, V_{DD33} = 3.3V	●	10	12.5	14.7	V
I_{VOUT_ENn}	Output Sourcing Current	V_{VOUT_ENn} Pull-Up Enabled, V_{VOUT_ENn} = 1V	●	–5	–6	–8	µA
	Output Sinking Current	Strong Pull-Down Enabled, V_{VOUT_ENn} = 0.4V	●	3	5	8	mA
		Weak Pull-Down Enabled, V_{VOUT_ENn} = 0.4V	●	33	50	60	µA
	Output Leakage Current	Internal Pull-Up Disabled, 0V ≤ V_{VOUT_ENn} ≤ 15V	●			±1	µA
V_{OUT} Enable Output (V_{OUT_EN} [7:4]) Characteristics							
I_{VOUT_ENn}	Output Sinking Current	Strong Pull-Down Enabled, V_{OUT_ENn} = 0.1V	●	3	6	9	mA
	Output Leakage Current	0V ≤ V_{VOUT_ENn} ≤ 6V	●			±1	µA
V_{IN} Enable Output (V_{IN_EN}) Characteristics							
V_{VIN_EN}	Output High Voltage	I_{VIN_EN} = –5µA, V_{DD33} = 3.3V	●	10	12.5	14.7	V
I_{VIN_EN}	Output Sourcing Current	V_{IN_EN} Pull-Up Enabled, V_{VIN_EN} = 1V	●	–5	–6	–8	µA
	Output Sinking Current	V_{VIN_EN} = 0.4V	●	3	5	8	mA
	Leakage Current	Internal Pull-Up Disabled, 0V ≤ V_{VIN_EN} ≤ 15V	●			±1	µA
EEPROM Characteristics							
Endurance	(Notes 6, 9)	0°C < T_J < 85°C During EEPROM Write Operations	●	10,000			Cycles
Retention	(Notes 6, 9)	T_J < 85°C	●	10			Years
t_{MASS_WRITE}	Mass Write Operation Time (Note 7)	STORE_USER_ALL, 0°C < T_J < 85°C During EEPROM Write Operations	●		440	4100	ms
Digital Inputs SCL, SDA, CONTROL0, CONTROL1, WDI/RESETB, FAULTB00, FAULTB01, FAULTB10, FAULTB11, WP							
V_{IH}	High Level Input Voltage		●	2.1			V
V_{IL}	Low Level Input Voltage		●			1.5	V
V_{HYST}	Input Hysteresis				20		mV
I_{LEAK}	Input Leakage Current	0V ≤ V_{PIN} ≤ 5.5V, SDA, SCL, CONTROL*n* Pins Only	●			±2	µA
		0V ≤ V_{PIN} ≤ V_{DD33} + 0.3V, FAULTB*zn*, WDI/RESETB, WP Pins Only	●			±2	µA
t_{SP}	Pulse Width of Spike Suppressed	FAULTB*zn*, CONTROL*n* Pins Only			10		µs
		SDA, SCL Pins Only			98		ns
t_{FAULT_MIN}	Minimum Low Pulse Width for Externally Generated Faults			110			ms
t_{RESETB}	Pulse Width to Assert Reset	$V_{WDI/RESETB}$ ≤ 1.5V	●	300			µs
t_{WDI}	Pulse Width to Reset Watchdog Timer	$V_{WDI/RESETB}$ ≤ 1.5V	●	0.3		200	µs

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