

NUP4304MR6, SZNUP4304MR6

Low Capacitance Diode Array for ESD Protection in Four Data Lines

NUP4304MR6 is a micro-integrated device designed to provide protection for sensitive components from possible harmful electrical transients; for example, ESD (electrostatic discharge).

Features

- Low Capacitance (1.5 pF Maximum Between I/O Lines)
- Single Package Integration Design
- Provides ESD Protection for JEDEC Standards JESD22
Machine Model = Class C
Human Body Model = Class 3B
- Protection for IEC61000-4-2 (Level 4)
8.0 kV (Contact)
15 kV (Air)
- Ensures Data Line Speed and Integrity
- Fewer Components and Less Board Space
- Direct the Transient to Either Positive Side or to the Ground

Applications

- USB 1.1 and 2.0 Data Line Protection
- T1/E1 Secondary IC Protection
- T3/E3 Secondary IC Protection
- HDSL, IDSL Secondary IC Protection
- Video Line Protection
- Microcontroller Input Protection
- Base Stations
- I²C Bus Protection
- AEC-Q101 Qualified and PPAP Capable
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements
- This is a Pb-Free Device*



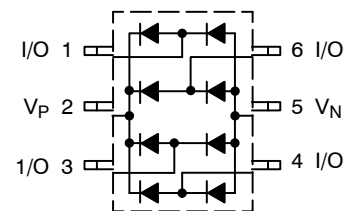
ON Semiconductor®

<http://onsemi.com>

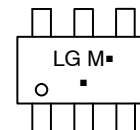


TSOP-6
CASE 318F

PIN CONFIGURATION AND SCHEMATIC



MARKING DIAGRAM



LG = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NUP4304MR6T1G	TSOP-6 (Pb-Free)	3,000 / Tape & Reel
SZNUP4304MR6T1G	TSOP-6 (Pb-Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NUP4304MR6, SZNUP4304MR6

MAXIMUM RATINGS (Each Diode) ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	70	Vdc
Forward Current	I_F	200	mAdc
Peak Forward Surge Current	$I_{FM(surge)}$	500	mAdc
Repetitive Peak Reverse Voltage	V_{RRM}	70	V
Average Rectified Forward Current (Note 1) (averaged over any 20 ms period)	$I_{F(AV)}$	715	mA
Repetitive Peak Forward Current	I_{FRM}	450	mA
Non-Repetitive Peak Forward Current t = 1.0 μs t = 1.0 ms t = 1.0 S	I_{FSM}	2.0 1.0 0.5	A

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. FR-5 = $1.0 \times 0.75 \times 0.062$ in.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	556	$^\circ\text{C/W}$
Lead Solder Temperature Maximum 10 Seconds Duration	T_L	260	$^\circ\text{C}$
Junction Temperature	T_J	-40 to +150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (Each Diode)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Reverse Breakdown Voltage ($I_{(BR)} = 100 \mu\text{A}$)	$V_{(BR)}$	70	-	-	Vdc
Reverse Voltage Leakage Current ($V_R = 70$ Vdc) ($V_R = 25$ Vdc, $T_J = 150^\circ\text{C}$) ($V_R = 70$ Vdc, $T_J = 150^\circ\text{C}$)	I_R	-	-	2.5 30 50	μAdc
Capacitance (between I/O pins) ($V_R = 0$ V, f = 1.0 MHz)	C_D	-	0.8	1.5	pF
Capacitance (between I/O pin and ground) ($V_R = 0$ V, f = 1.0 MHz)	C_D	-	1.6	3	pF
Forward Voltage ($I_F = 1.0$ mAdc) ($I_F = 10$ mAdc) ($I_F = 50$ mAdc) ($I_F = 150$ mAdc)	V_F	-	-	715 855 1000 1250	mV _{dc}

1. FR-5 = $1.0 \times 0.75 \times 0.062$ in.

2. Alumina = $0.4 \times 0.3 \times 0.024$ in. 99.5% alumina.

NUP4304MR6, SZNUP4304MR6

Curves Applicable to Each Cathode

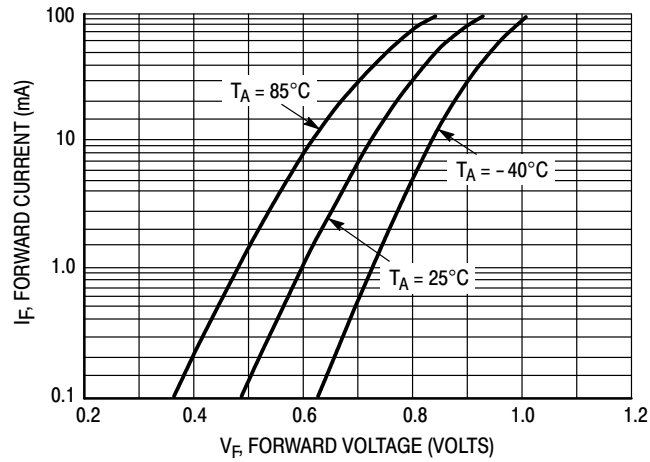


Figure 1. Forward Voltage

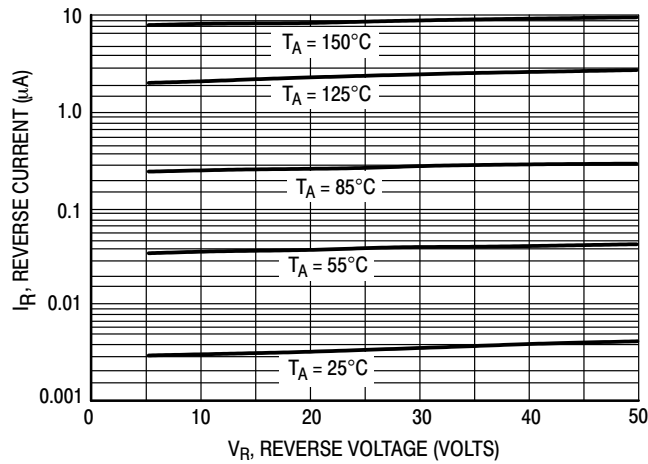


Figure 2. Leakage Current

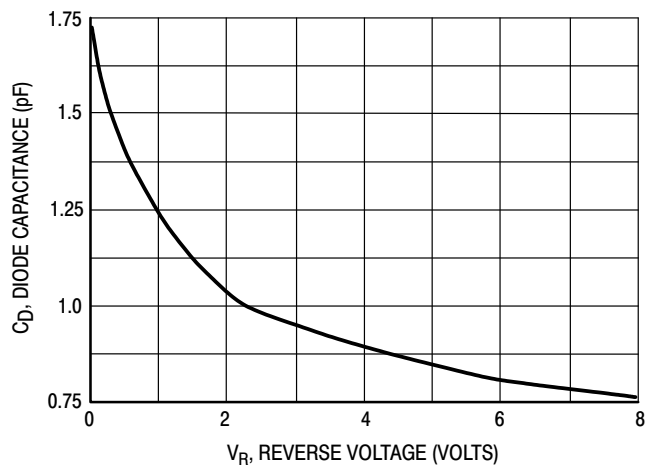


Figure 3. Capacitance

APPLICATIONS INFORMATION

The NUP4304MR6 is a low capacitance diode array designed to protect sensitive electronics such as communications systems, computers, and computer peripherals against damage due to ESD events or transient overvoltage conditions. Because of its low capacitance, it can be used on high speed I/O data lines. The integrated design of the NUP4304MR6 offers surge rated, low capacitance steering diodes integrated in a single package (TSOP-6). If a transient condition occurs, the steering diodes will drive the transient to the positive rail of the power supply or to ground.

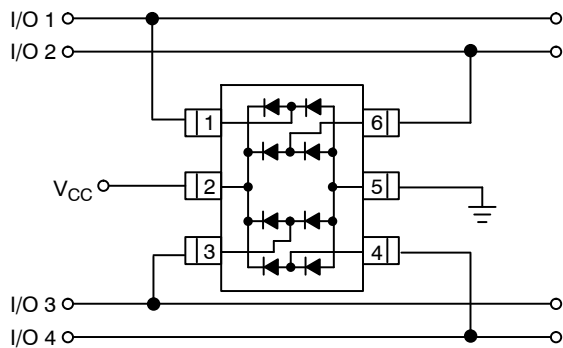
NUP4304MR6 Configuration Options

The NUP4304MR6 is able to protect up to four data lines against transient overvoltage conditions by driving them to a fixed reference point for clamping purposes. The steering diodes will be forward biased whenever the voltage on the protected line exceeds the reference voltage (V_f or $V_{CC}+V_f$). The diodes will force the transient current to bypass the sensitive circuit.

Data lines are connected at pins 1, 3, 4 and 6. The negative reference is connected at pin 5. This pin must be connected directly to ground by using a ground plane to minimize the PCB's ground inductance. It is very important to reduce the PCB trace lengths as much as possible to minimize parasitic inductance.

Option 1

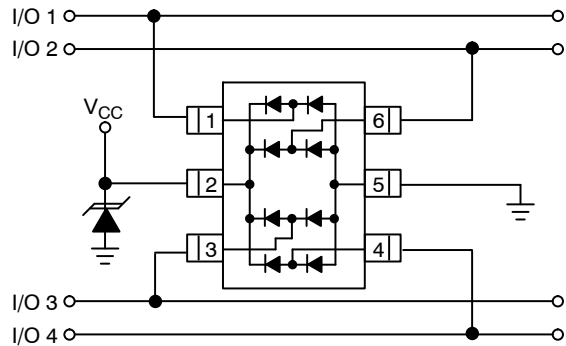
Protection of four data lines using V_{CC} as reference.



For this configuration, connect pin 2 directly to the positive supply rail (V_{CC}), the data lines are referenced to the supply voltage. Biasing of the steering diodes reduces their capacitance.

Option 2

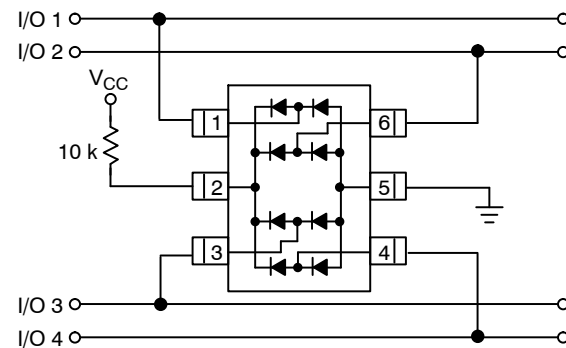
Protection of four data lines and the supply rail using V_{CC} as a reference and an external TVS diode.



If additional protection of the supply rail is desired, an external TVS diode may be added across V_{CC} and ground. This will prevent overvoltage conditions on the supply rail protecting the supply and other circuits connected to it.

Option 3

Protection of four data lines with bias and power supply isolation resistor.

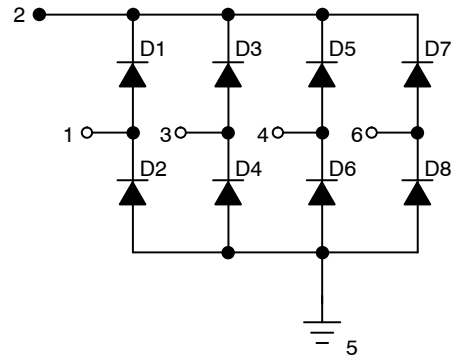
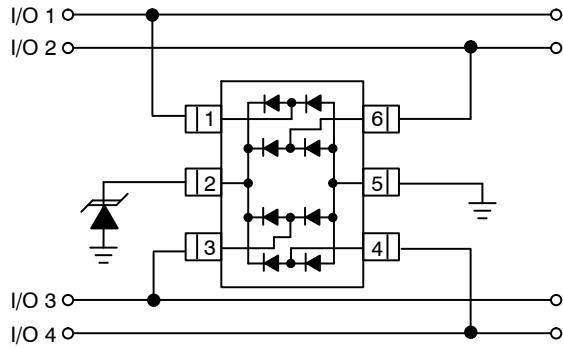


The NUP4304MR6 can be isolated from the power supply by connecting a series resistor between pin 2 and V_{CC} . A 10 kΩ resistor is recommended for this application. This will maintain bias on the internal steering diodes, reducing their capacitance.

NUP4304MR6, SZNUP4304MR6

Option 4

Protection of four data lines without biasing of the internal steering diodes.



NUP4304MR6 Equivalent Circuit

In applications lacking a positive supply reference an external TVS diode may be used as a reference. For these applications, the TVS is connected between pin 2 and the ground plane. The steering diodes will conduct whenever the voltage on the protected line exceeds their forward voltage plus the working voltage of the TVS diode ($V_c = V_f + V_{TVS}$). In this case, the effective capacitance of the steering diodes will be higher than if a bias was applied.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

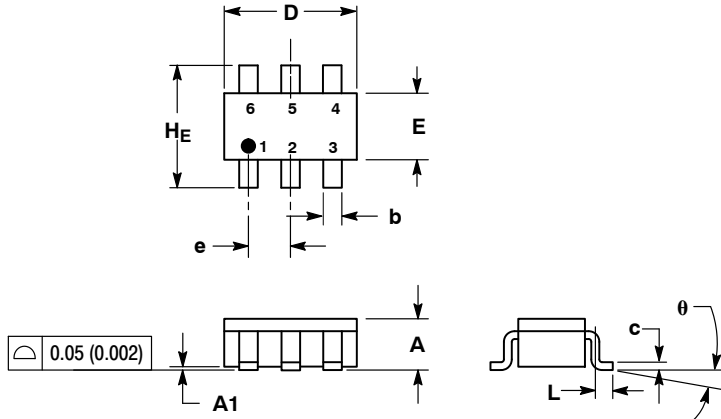
ON Semiconductor®



SC-74 CASE 318F-05 ISSUE N

DATE 08 JUN 2012

SCALE 2:1

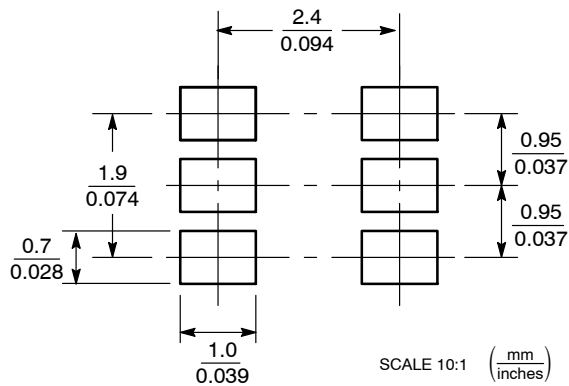


NOTES:

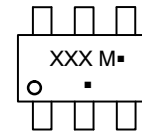
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318F-01, -02, -03, -04 OBSOLETE. NEW STANDARD 318F-05.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.37	0.50	0.010	0.015	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
HE	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	-	10°	0°	-	10°

SOLDERING FOOTPRINT*



GENERIC MARKING DIAGRAM*



- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

- | | | | | | |
|--|---|--|---|--|--|
| <p>STYLE 1:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE</p> | <p>STYLE 2:
PIN 1. NO CONNECTION
2. COLLECTOR
3. EMITTER
4. NO CONNECTION
5. COLLECTOR
6. BASE</p> | <p>STYLE 3:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1</p> | <p>STYLE 4:
PIN 1. COLLECTOR 2
2. EMITTER 1/EMITTER 2
3. COLLECTOR 1
4. EMITTER 3
5. BASE 1/BASE 2/COLLECTOR 3
6. BASE 3</p> | <p>STYLE 5:
PIN 1. CHANNEL 1
2. ANODE
3. CHANNEL 2
4. CHANNEL 3
5. CATHODE
6. CHANNEL 4</p> | <p>STYLE 6:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE</p> |
| <p>STYLE 7:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1</p> | <p>STYLE 8:
PIN 1. EMITTER 1
2. BASE 2
3. COLLECTOR 2
4. EMITTER 2
5. BASE 1
6. COLLECTOR 1</p> | <p>STYLE 9:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2</p> | <p>STYLE 10:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE</p> | <p>STYLE 11:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR</p> | |

DOCUMENT NUMBER:	98ASB42973B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SC-74	PAGE 1 OF 1

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

ON Semiconductor Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:
Voice Mail: 1 800-282-9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative