SBAS128B – JANUARY 2000 – REVISED MAY 2007

SoundPLUS™ Stereo Audio DIGITAL-TO-ANALOG CONVERTER with VCXO and PLL

FEATURES

- **COMPLETE DELTA-SIGMA STEREO DAC**
- **VOLTAGE-CONTROLLED CRYSTAL OSCILLATOR: 27MHz ±150ppm Output with 0V to 3V Input**
- **PROGRAMMABLE PLL 256f_S or 384f_S Audio System Clock Output**
- **DYNAMIC PERFORMANCE: Dynamic Range: 94dB SNR: 94dB THD+N: –89dB**
- **SAMPLING FREQUENCIES: 16kHz, 22.05kHz, 24kHz 32kHz, 44.1kHz, 48kHz 64kHz, 88.2kHz, 96kHz**
- **SERIAL AUDIO INTERFACE: Standard or I²S™ Data Formats 16-, 20-, or 24-Bit Data**
- **I²C-BUS™ INTERFACE FOR CONTROL REGISTERS: Slave Receiver Operation 7-Bit Addressing Standard Transfer Rate (up to 100kbps)**
- **PROGRAMMABLE CONTROLS: Digital Attenuation (256 steps) Soft Mute Infinite Zero Detect Mute De-Emphasis (32kHz, 44.1kHz, 48kHz) DAC Output Mode**
- **SINGLE +5V SUPPLY**
- **SMALL SSOP-24 PACKAGE**

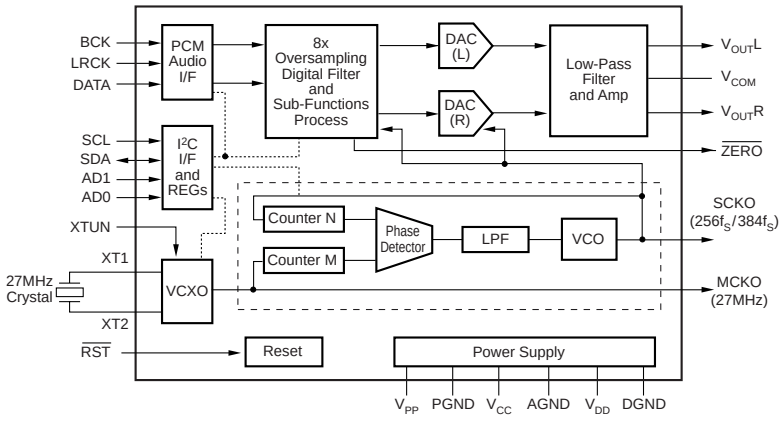
APPLICATIONS

- **SET-TOP BOXES**
- **DIGITAL BROADCAST RECEIVERS**

DESCRIPTION

The PCM1740 is a complete stereo audio digital-to-analog converter with on-chip PLL and VCXO. The PCM1740 is designed specifically for set-top box applications requiring high-quality audio playback, a precision tuned 27MHz master clock source, and support for multiple audio-sampling frequencies.

The stereo digital-to-analog converter (DAC) uses multi-bit, delta-sigma architecture, which includes an 8x interpolation filter, 3rd-order noise shaping, 5-level amplitude quantization, and an analog low-pass filter. The PCM1740 includes a number of user-programmable functions, which are accessed via a standard I²C-Bus interface.



ABSOLUTE MAXIMUM RATINGS(1)

Power Supply Voltage(2)	+6.5V
Supply Voltage Differences(3)	±0.1V
GND Voltage Differences(4)	±0.1V
Digital Input Voltage	–0.3V to (V_{DD} + 0.3V)
Analog Input Voltage	–0.3V to (V_{CC} + 0.3V)
Input Current (any pins except supplies)	±10mA
Operating Temperature Range	–25°C to +85°C
Storage Temperature	–55°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 5s)	+260°C
Package Temperature (IR reflow, peak, 10s)	+235°C

NOTES: (1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability. (2) V_{CC}, V_{DD}, V_{PP}. (3) Among V_{CC}, V_{DD}, V_{PP}. (4) Among AGND, DGND, and PGND.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

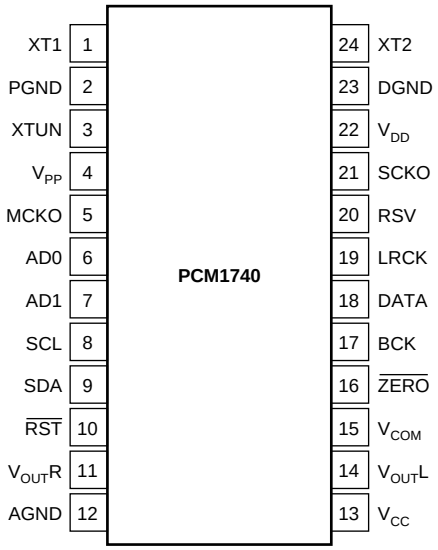
PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
PCM1740E	SSOP-24	DB	–25°C to +85°C	PCM1740E	PCM1740E	Rails, 58
"	"	"	"	PCM1740E	PCM1740E/2K	Tape and Reel, 2000

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com.

PIN CONFIGURATION

Top View **SSOP**



PIN ASSIGNMENTS

PIN	NAME	I/O	FUNCTION
1	XT1	—	27MHz Crystal connection.
2	PGND	—	PLL and VCXO ground.
3	XTUN	IN	VCXO tune, tuning voltage range from 0V to 3V.
4	V_{PP}	—	PLL and VCXO power supply, +5V.
5	MCKO	OUT	Buffered clock output of VCXO.
6	AD0	IN	Device address pin for I^2C-BUS.(1)
7	AD1	IN	Device address pin for I^2C-BUS.(1)
8	SCL	IN	Bit clock input for I^2C-BUS interface.
9	SDA	IN/OUT	Serial data for I^2C-BUS interface.
10	$\overline{RST}$	IN	Reset, active LOW.(2)
11	$V_{OUT}R$	OUT	Right-channel analog voltage output.
12	AGND	—	Analog ground.
13	V_{CC}	—	Analog power supply, +5V.
14	$V_{OUT}L$	OUT	Left-channel analog voltage output.
15	V_{COM}	—	DC common-mode voltage output.
16	$\overline{ZERO}$	OUT	Zero flag output, active LOW.(3)
17	BCK	IN	Bit clock input for serial audio data.(1)
18	DATA	IN	Serial audio data input.(1)
19	LRCK	IN	Left and right word clock, equal to the sampling rate (f_S).(1)
20	RSV	—	Reserved must be open.
21	SCKO	OUT	System clock output, 256/384 f_S.
22	V_{DD}	—	Digital power supply, +5V.
23	DGND	—	Digital ground.
24	XT2	—	27MHz Crystal connection.

NOTES: (1) Schmitt trigger input.
(2) Schmitt trigger input with internal pull-up resistor.
(3) Open drain output.

ELECTRICAL CHARACTERISTICS

All specifications at T_A = +25°C, V_{CC} = V_{DD} = V_{PP} = 5.0V, f_S = 44.1kHz, system clock = 384f_S, 16-bit data, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1740E MIN	PCM1740E TYP	PCM1740E MAX	UNITS
RESOLUTION			16		Bits
DATA FORMAT					
Audio Interface Format			Standard/I²S Selectable		
Audio Data Bit Length			16/20/24 Selectable		Bits
Audio Data Format			MSB First, Two's Binary Complement		
Sampling Frequency (f_S)	Standard (f_S)	32	44.1	48	kHz
	Half (f_S)	16	22.05	24	kHz
	Double (f_S)	64	88.2	96	kHz
Internal System Clock Frequency			256f_S/384f_S		
DIGITAL INPUT/OUTPUT					
Logic Family	Input Logic		TTL Compatible		
High Level Input Voltage: V_{IH}(1), (2)		2.0			VDC
Low Level Input Voltage: V_{IL}(1), (2)				0.8	VDC
High Level Input Current: I_{IH}(1), (2)	V_{IH} = V_{DD}			±10	µA
Low Level Input Current:					
I_{IL}(1)	V_{IL} = 0V			±10	µA
I_{IL}(2)	V_{IL} = 0V			–120	µA
High Level Output Voltage: V_{OH}(3)	I_{OH} = –2mA	V_{DD} – 0.5V			VDC
Low Level Output Voltage:					
V_{OL}(3)	I_{OL} = 4mA			0.5	VDC
V_{OL}(4)	I_{OL} = 2mA			0.5	VDC
DIGITAL INPUT/OUTPUT of I²C-BUS INTERFACE					
High Level Input Voltage: V_{IH}(5)		3.0			V
Low Level Input Voltage: V_{IL}(5)		–0.3		1.5	V
Low Level Output Voltage: V_{OL}(6)		0		0.4	V
Output Fall Time: t_{OF}(7)				250	ns
Input Logic Current: I_I(8)	10% to 90% of V_{DD}	–10		10	µA
Capacitance for each I/O pin: C_I(5)				10	pF
VCXO CHARACTERISTICS (MCKO)	27MHz, Fundamental Crystal				
Crystal Clock Frequency(9)			27.0000		MHz
Crystal Clock Accuracy(9)			±30		ppm
XTUN Tuning Voltage Range(10)		0		3.0	V
XTUN Input Impedance(10)			60		kΩ
Output Clock Frequency	XTUN = 1.3V		27.0000		MHz
Output Clock Accuracy	XTUN = 1.3V		±50		ppm
VCXO Tuning Range	XTUN = 0V – 3V		300		ppm
Output Clock Duty Cycle	10pF Load	35	45	55	%
Output Clock Jitter	Standard Deviation		100		ps
Output Rise Time	20% to 80% V_{DD}, 10pF Load		4		ns
Output Fall Time	80% to 20% V_{DD}, 10pF Load		4		ns
Response Time(11)				10	µs
Power Up Time(12)				5	ms
PLL AC CHARACTERISTICS (SCKO)					
Output Clock Frequency	MCKO = 27.0MHz	4.096		36.864	MHz
Output Clock Duty Cycle	10pF Load	40	50	60	%
Output Clock Jitter	Standard Deviation		150		ps
Output Rise Time	20% to 80% V_{DD}, 10pF Load		4		ns
Output Fall Time	80% to 20% V_{DD}, 10pF Load		4		ns
Frequency Transition Time(13)				20	ms
Power Up Time(14)			15	30	ms
DYNAMIC PERFORMANCE(15)					
THD+N:					
V_{OUT} = 0dB	f_S = 44.1kHz		0.0035	0.01	%
	f_S = 96kHz		0.007		%
V_{OUT} = –60dB	f_S = 44.1kHz		0.0035	0.01	%
	f_S = 96kHz		0.007		%
Dynamic Range	f_S = 44.1kHz, EIAJ, A-Weighted	90	94		dB
	f_S = 96kHz, A-Weighted		90		dB
Signal-to-Noise Ratio(16)	f_S = 44.1kHz, EIAJ, A-weighted	90	94		dB
	f_S = 96kHz, A-weighted		90		dB
Channel Separation	f_S = 44.1kHz	88	92		dB
	f_S = 96kHz		88		dB
Level Linearity Error	V_{OUT} = –90dB		±1.0		dB

ELECTRICAL CHARACTERISTICS (Cont.)

All specifications at T_A = +25°C, V_{CC} = V_{DD} = V_{PP} = 5.0V, f_S = 44.1kHz, system clock = 384f_S, 16-bit data, unless otherwise noted.

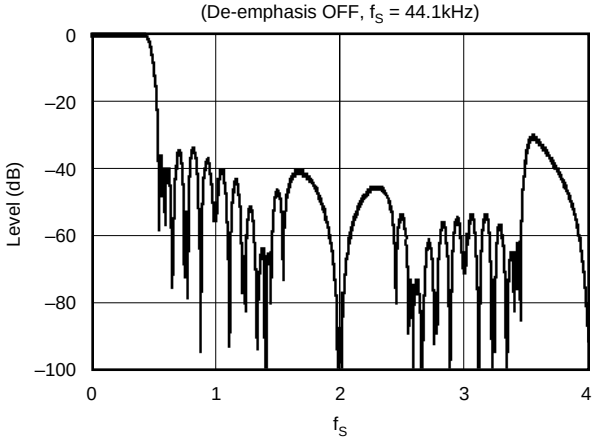
PARAMETER	CONDITIONS	PCM1740E MIN	PCM1740E TYP	PCM1740E MAX	UNITS
DC ACCURACY					
Gain Error			±1.0	±3.0	% of FSR
Gain Mismatch, Channel-to-Channel			±1.0	±3.0	% of FSR
Bipolar Zero Error			±1.0		% of FSR
ANALOG OUTPUT					
Voltage Range	Full Scale (0dB)		0.62 V_{CC}		V_{PP}
Center Voltage			0.5 V_{CC}		VDC
Load Impedance	AC Coupled	5			kΩ
DIGITAL FILTER PERFORMANCE					
Passband				0.445 f_S	Hz
Stop Band		0.555 f_S			Hz
Passband Ripple				±0.17	dB
Stop Band Attenuation		–35			dB
De-Emphasis Error		–0.2		+0.55	dB
Delay Time			11.125/f_S		sec
ANALOG FILTER PERFORMANCE					
Frequency Response	20Hz to 20kHz		–0.16		dB
	20Hz to 40kHz		–0.6		dB
POWER SUPPLY REQUIREMENTS					
Voltage Range	V_{DD}, V_{CC}, V_{PP}	+4.5	+5	+5.5	VDC
Supply Current, I_{DD} + I_{CC} + I_{PP}	V_{DD} = V_{CC} = V_{PP} = +5V		25	30	mA
Power Dissipation	V_{DD} = V_{CC} = V_{PP} = +5V		125	150	mW
TEMPERATURE RANGE					
Operation		–25		+85	°C
Storage		–55		+125	°C
Thermal Resistance, θ_{JA}			100		°C/W

NOTES: (1) Pins 6, 7, 18, 19: AD0, AD1, BCK, DATA, LRCK (Schmitt trigger input).
(2) Pin 10: $\overline{RST}$ (Schmitt trigger input with internal pull-up resistor).
(3) Pins 5, 21: MCKO, SCKO. (4) Pin 16: $\overline{ZERO}$ (open drain output).
(5) Pins 8, 9: SCL, SDA.
(6) Pin 9: SDA (open drain output, I_{OL} = 3mA).
(7) Pin 9: SDA (from V_{IHMIN} to V_{ILMAX} with a bus capacitance from 10pF to 400pF).
(8) Pins 8, 9: SCL, SDA (input current each I/O pin with an input voltage between 0.1V_{DD} and 0.9V_{DD}).
(9) This characteristic is the requirement for crystal oscillator.
(10) Pin 3: XTUN.
(11) The maximum response time when the XTUN is changed.
(12) The maximum delay time from power on to oscillation.
(13) The maximum lock up time when the PLL frequency is changed.
(14) The maximum delay time from power on to lock up.
(15) Dynamic performance specifications are tested with a 20kHz low-pass filter using a Shibasoku distortion analyzer 725°C with 30kHz LPF, 400Hz HPF, Average-Mode.
(16) SNR is tested with infinite zero detection circuit disabled.

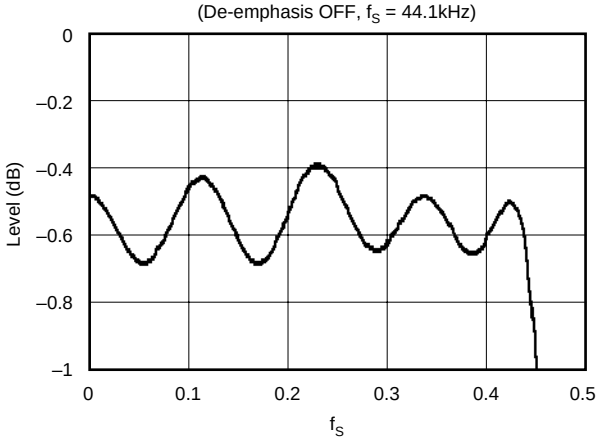
TYPICAL CHARACTERISTICS

At T_A = +25°C, V_{CC} = V_{DD} = +5V, f_S = 44.1kHz, f_{SCKO} = 384f_S = 16.9344MHz, and 16-bit data, unless otherwise noted.

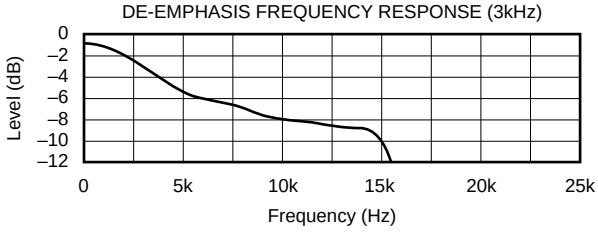
FREQUENCY RESPONSE
(De-emphasis OFF, f_S = 44.1kHz)



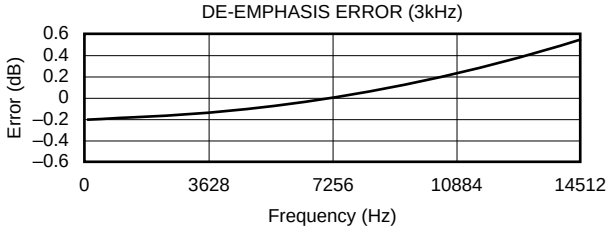
PASSBAND RIPPLE
(De-emphasis OFF, f_S = 44.1kHz)



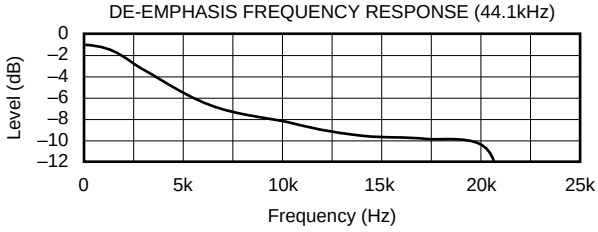
DE-EMPHASIS FREQUENCY RESPONSE (3kHz)



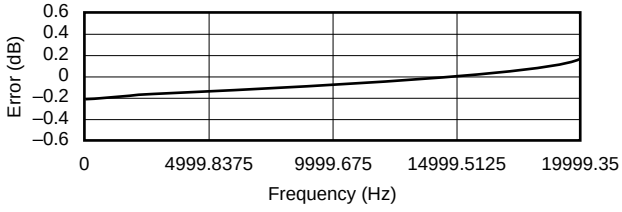
DE-EMPHASIS ERROR (3kHz)



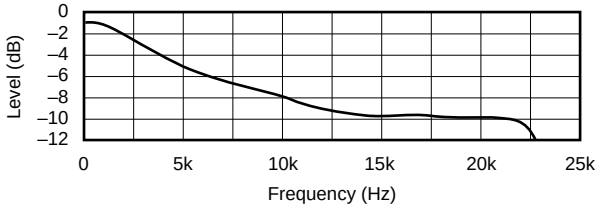
DE-EMPHASIS FREQUENCY RESPONSE (44.1kHz)



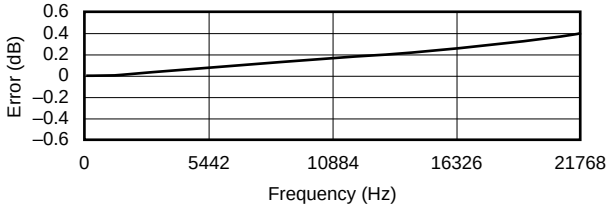
DE-EMPHASIS ERROR (44.1kHz)



DE-EMPHASIS FREQUENCY RESPONSE (48kHz)



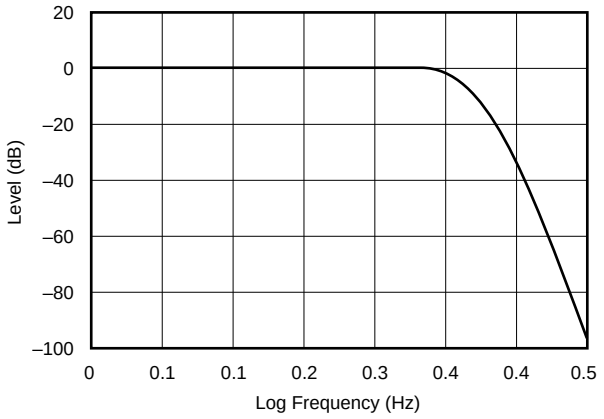
DE-EMPHASIS ERROR (48kHz)



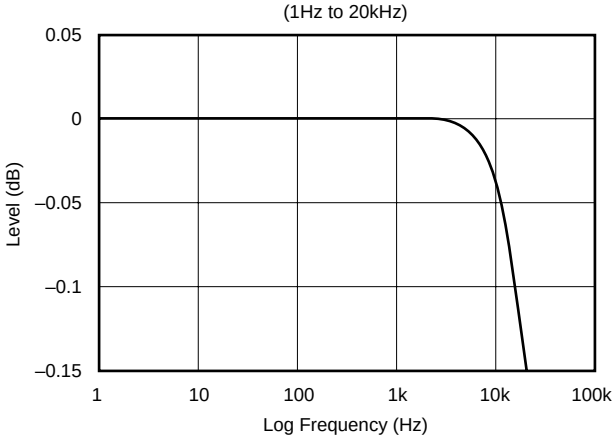
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_{CC} = V_{DD} = +5V, f_S = 44.1kHz, F_{SCKO} = 384f_S = 16.9344MHz, and 16-bit data, unless otherwise noted.

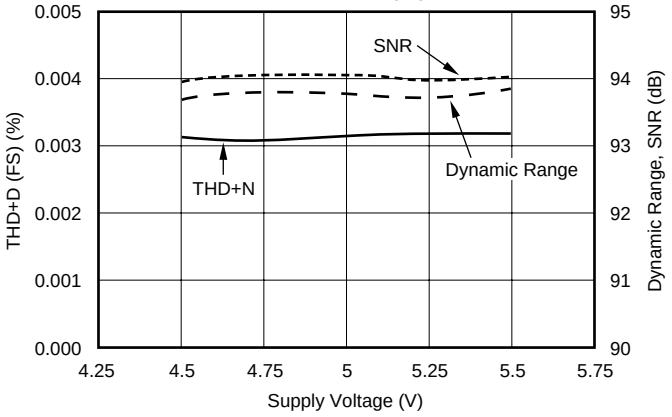
ANALOG FILTER
(1Hz to 10MHz)



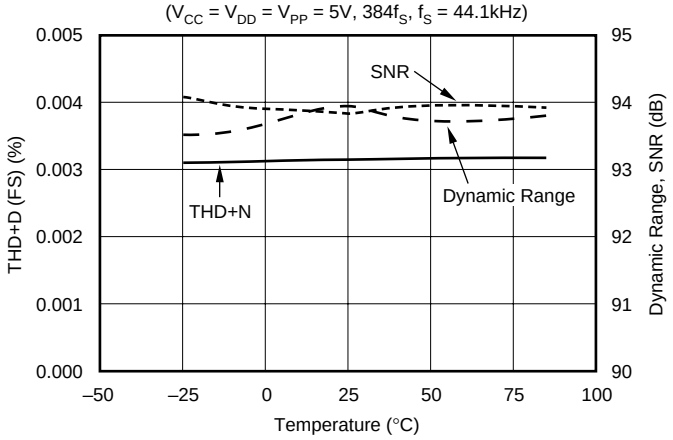
ANALOG FILTER
(1Hz to 20kHz)



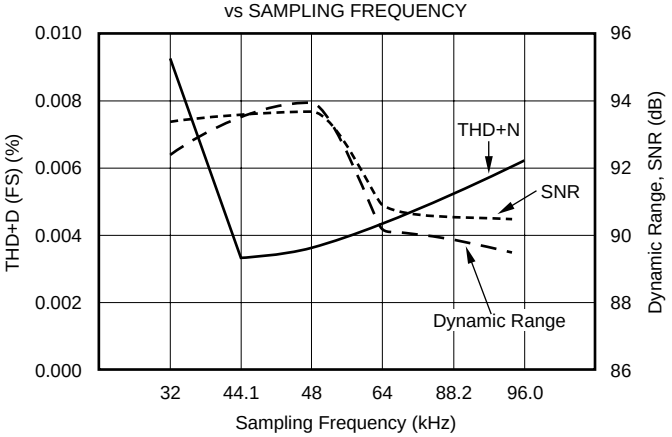
THD+N (FS), DYNAMIC RANGE, and SNR
vs SUPPLY VOLTAGE
(Temperature = 25°C, 384f_S, f_S = 44.1kHz)



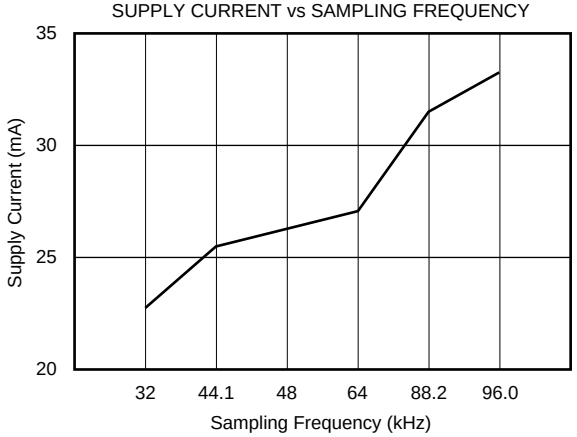
THD+N (FS), DYNAMIC RANGE, and SNR
vs TEMPERATURE
(V_{CC} = V_{DD} = V_{PP} = 5V, 384f_S, f_S = 44.1kHz)



THD+N (FS), DYNAMIC RANGE, and SNR
vs SAMPLING FREQUENCY



SUPPLY CURRENT vs SAMPLING FREQUENCY



STEREO DIGITAL-TO-ANALOG CONVERTER

The stereo DACs of the PCM1740 use a multi-level delta-sigma architecture. Based upon a 3rd-order noise shaper and a 5-level amplitude quantizer, this section converts the 8x oversampled, 18-bit input data from the interpolation filter to a 5-level delta-sigma format. A block diagram of the multi-level delta-sigma modulator is shown in Figure 1. This architecture has the advantage of improved stability and increased tolerance to clock jitter when compared to the one-bit (2-level) delta-sigma DACs.

The combined oversampling rate of the delta-sigma modulator and the 8x interpolation filter is $48f_S$ for a $384f_S$ system clock, and $64f_S$ for a $256f_S$ system clock. The theoretical quantization noise performance for the 5-level delta-sigma modulator is shown in Figure 2.

The output of the delta-sigma modulator is low-pass filtered and buffered by an on-chip output amplifier. For best performance, an external low-pass filter is recommended. Refer to the *Applications Information* section of this data sheet for details regarding DAC output filter recommendations.

The PCM1740 includes two analog outputs, $V_{OUT}L$ (pin 14) and $V_{OUT}R$ (pin 11), corresponding to the left and right audio outputs. The full-scale output amplitude is $0.62 \times V_{CC}$, or $3.1V_{PP}$ with a +5V supply and an AC-coupled load of 5kΩ or greater. The analog outputs are centered about the DC common-mode voltage, which is typically $V_{CC}/2$.

The DC common-mode voltage is made available at the V_{COM} output (pin 15). This is an unbuffered output, primarily used for decoupling purposes. See the *Applications Information* section of this data sheet for more information regarding the use of the V_{COM} output for biasing external circuitry.

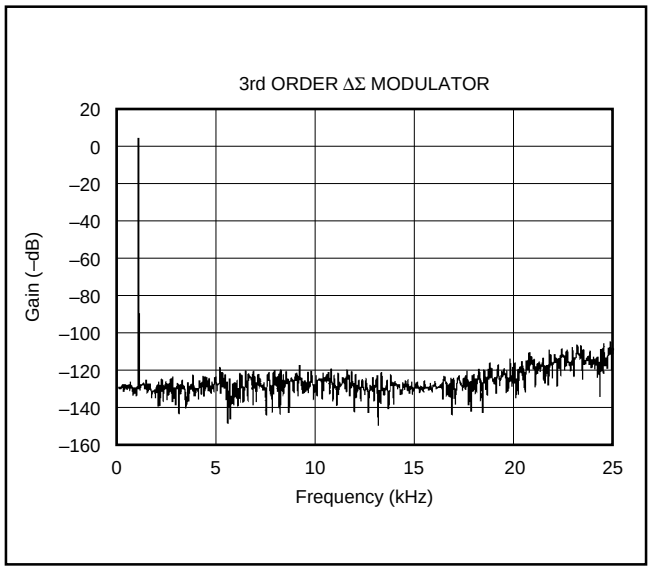


FIGURE 2. Quantization Noise Spectrum.

VOLTAGE CONTROLLED CRYSTAL OSCILLATOR (VCXO)

The PCM1740 includes an on-chip voltage-controlled crystal oscillator, or VCXO, which is used to generate the 27MHz master clock required by most digital broadcast and MPEG-2 decoding applications.

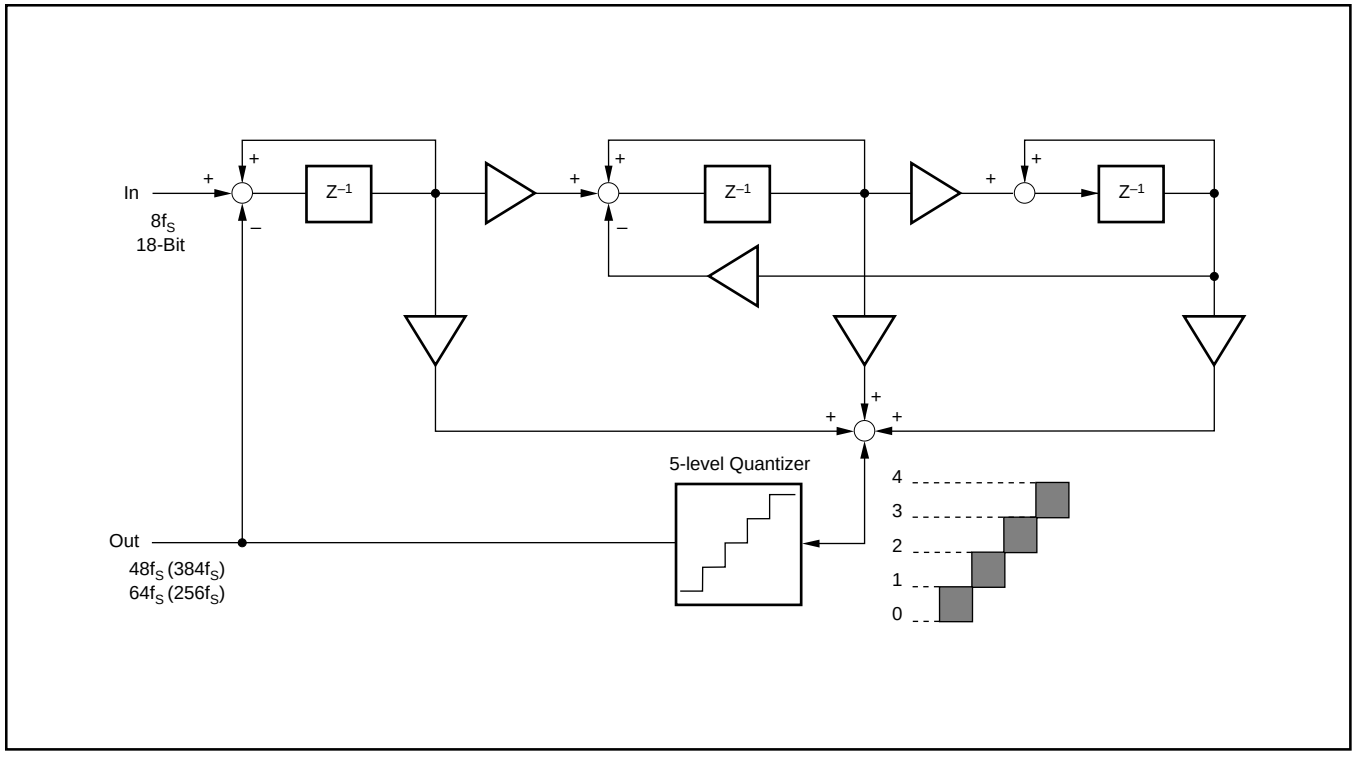


FIGURE 1. 5-Level ΔΣ Modulator Block Diagram.

The 27MHz clock is available at the MCKO output (pin 5). The VCXO output frequency can be precisely tuned using a control voltage at the XTUN input (pin 3). The tuning range is 27MHz ±150ppm typical for a 0V to +3V control voltage range. Figure 3 shows the VCXO equivalent circuit, while Figure 4 shows the typical tuning curve.

At power up, the VCXO requires 5ms start up time. The VCXO also exhibits a 10µs settling time in response to changes in the XTUN control voltage. VCXO operation and the MCKO output are not affected by the power on or external reset functions, continuing to operate during the initialization sequence.

Crystal Selection

The VCXO connects to an external 27MHz crystal via XT1 (pin 1) and XT2 (pin 24). The crystal should be AT-cut, fundamental mode with ±30ppm accuracy and less than 50Ω motional resistance. Crystal shunt capacitance should be 3pF maximum, while load capacitance should be less than 7pF. Miniature lead type or surface-mount devices are recommended. External load capacitors are not needed, since they are provided on-chip. The crystal should be placed as close as possible to the XT1 and XT2 pins to reduce effects of parasitic capacitance and land resistance.

PROGRAMMABLE PHASE LOCKED LOOP (PLL)

The PCM1740 includes an on-chip PLL for generating a $256f_S$ or $384f_S$ audio system clock from the 27MHz VCXO output. A block diagram of the PLL section is shown in Figure 5. The PLL output clock is used by the digital filter and delta-sigma modulator circuitry, and is made available at the SCKO output (pin 21) for use with additional audio converters and signal processors.

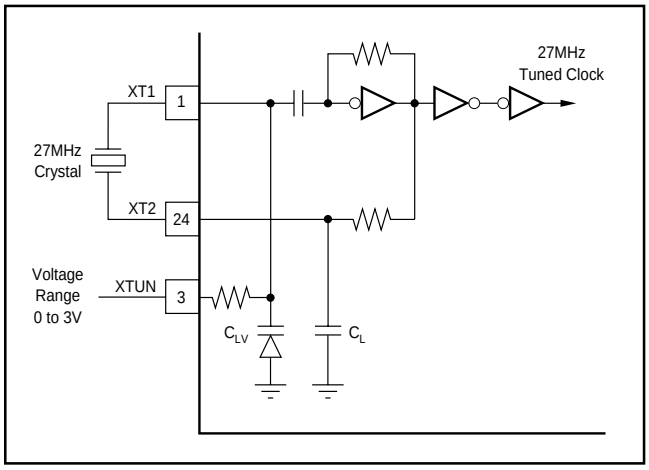


FIGURE 3. VCXO Equivalent Circuit.

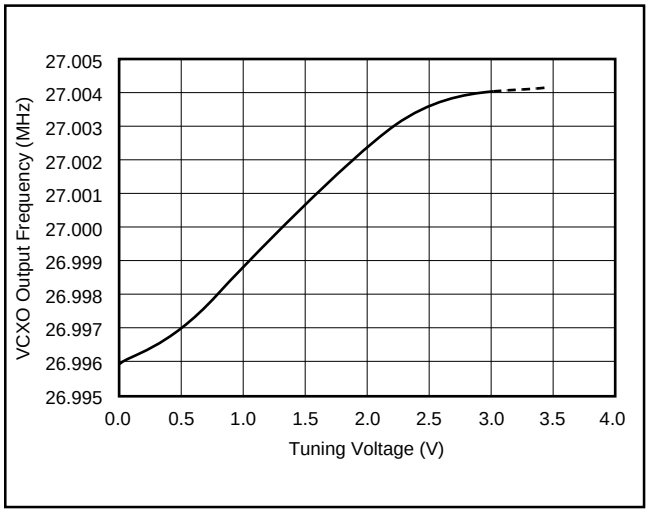


FIGURE 4. VCXO Output Frequency (MCKO) versus Tuning Voltage (XTUN).

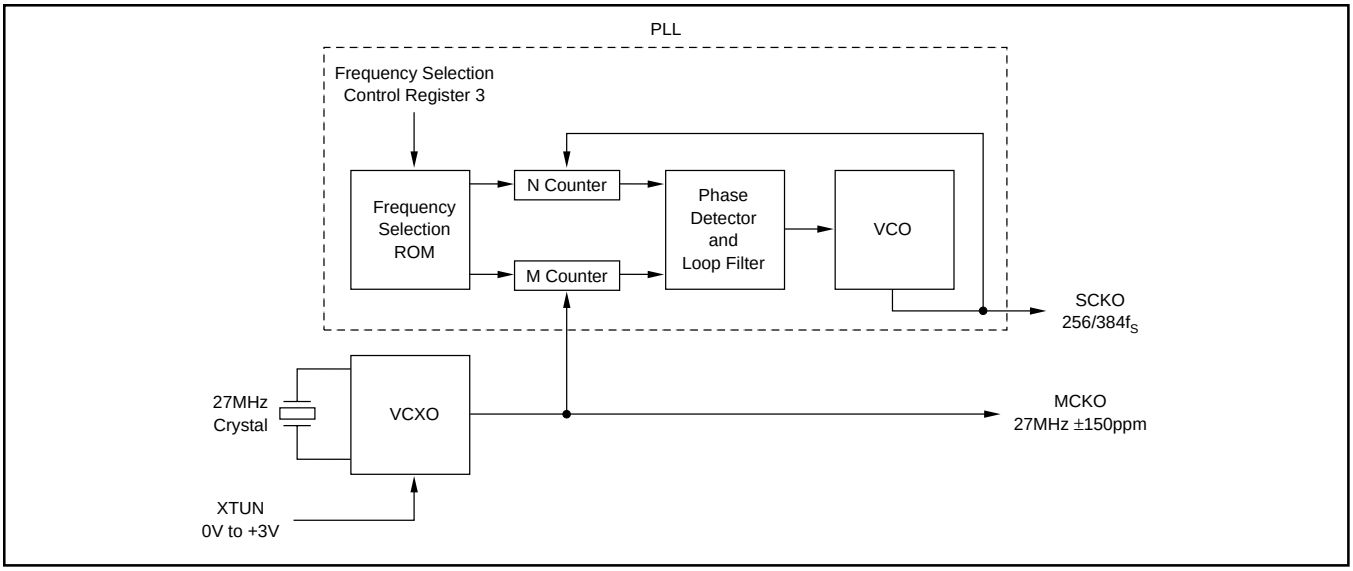


FIGURE 5. PLL Block Diagram.

The PLL can generate one of nine pre-programmed system clock rates for either $256f_S$ or $384f_S$ output. The PLL output and sampling frequencies are programmed using Control Register 3. Table I shows the available sampling frequencies and the corresponding PLL output clock rates. The reset default condition for the PLL is f_S = 44.1kHz with SCKO = $384f_S$, or 16.9344MHz.

SAMPLING FREQUENCY (LRCK)		INTERNAL SYSTEM Clock - $256f_S$	INTERNAL SYSTEM Clock - $384f_S$
16kHz	Half	4.096MHz	6.144MHz
32kHz	Normal	8.192MHz	12.288MHz
64kHz	Double	16.384MHz	24.576MHz
22.05kHz	Half	5.6448MHz	8.4672MHz
44.1kHz	Normal	11.2896MHz	16.9344MHz
88.2kHz	Double	22.5792MHz	33.8688MHz
24kHz	Half	6.144MHz	9.216MHz
48kHz	Normal	12.288MHz	18.432MHz
96kHz	Double	24.576MHz	36.864MHz

TABLE I. PLL Sampling and System Clock Frequencies.

At power-up, the PLL requires 30ms start up time for stabilization. The PLL also exhibits a settling time of 20ms in response to changes in sampling frequency selection. The PLL output continues to operate during power-on or external reset sequences, with the sampling frequency set to f_S = 44.1kHz and SCKO = $384f_S$.

RESET OPERATION

POWER-ON RESET

The PCM1740 includes power-on reset circuitry for start up initialization. The initialization sequence starts when V_{DD} exceeds 2.2V (typical). The initialization sequence requires 1024 PLL output (or SCKO) clock cycles for completion. During initialization, both $V_{OUT}L$ and $V_{OUT}R$ are forced to $V_{CC}/2$. Figure 6 shows the power-on reset timing, while Table II shows the reset default settings for user-programmable functions. The user should not attempt to write control registers via the I^2C-Bus interface during the initialization sequence.

EXTERNAL RESET

The PCM1740 includes an external reset input, $\overline{RST}$ (pin 10). This input may be used to force an initialization sequence. As shown in Figure 7, the $\overline{RST}$ pin must be held low for a minimum of 20ns. The initialization sequence will then start on the rising edge of $\overline{RST}$. Initialization requires 1024 PLL output (or SCKO) clock cycles for completion. During initialization, both $V_{OUT}L$ and $V_{OUT}R$ are forced to $V_{CC}/2$. Table II shows the reset default settings for user-programmable functions. The user should not attempt to write control registers via the I^2C-Bus interface during the initialization sequence.

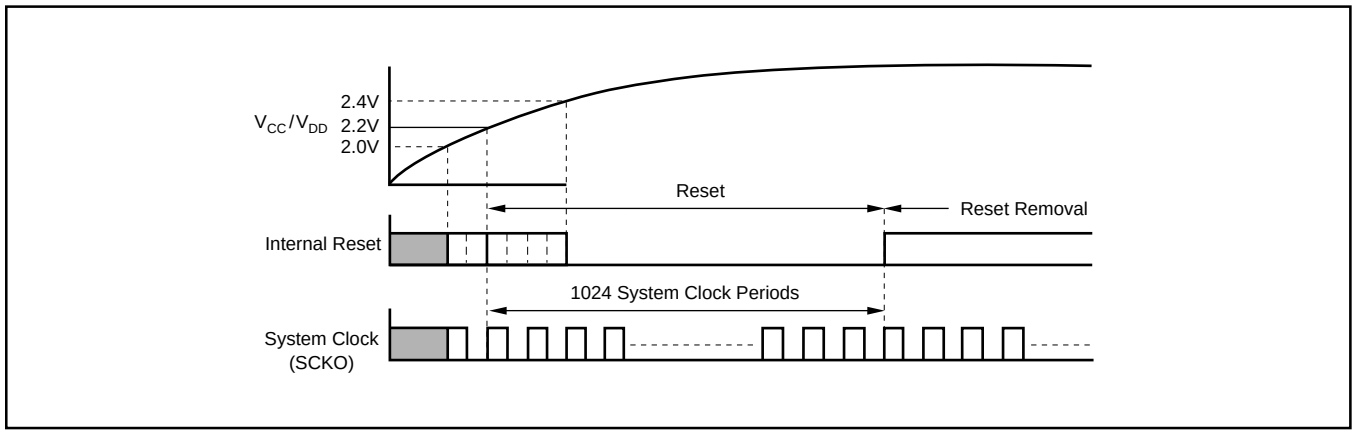


FIGURE 6. Power-On Reset Operation.

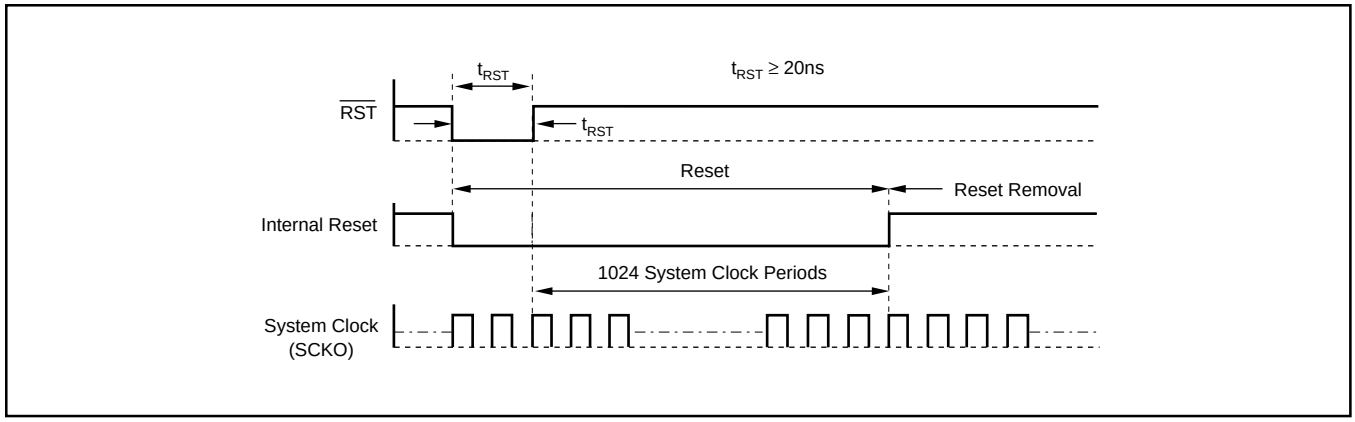


FIGURE 7. External Reset Operation.

ZERO FLAG OUTPUT

The PCM1740 includes a zero flag output, $\overline{ZERO}$ (pin 16). This is an open-drain output, and a 10kΩ pull-up resistor connected to V_{DD} is recommended when using the $\overline{ZERO}$ flag as a logic output.

The PCM1740 includes an infinite zero detection function that monitors the audio data at the DATA input (pin 18). If the audio data for both the left and right channels is all zeros for 65,536 continuous BCK clock cycles, the zero flag will be activated, turning on a MOSFET switch and connecting the $\overline{ZERO}$ pin to ground. This provides an active low output that may be used to control an external mute circuit, or as a logic indicator for an audio DSP/decoder or microprocessor.

AUDIO SERIAL INTERFACE

The PCM1740 includes a three-wire serial audio interface. This includes LRCK (pin 19), BCK (pin 17), and DATA (pin 18). The LRCK input is the audio left/right clock, which is used as a latch signal for the interface. The BCK input is used to clock audio data into the serial port. The DATA input carries multiplexed data for the left and right audio channels. Audio data must be Two's Complement, MSB first formatted. Figure 8 shows the typical connection between the PCM1740 audio serial interface and an audio DSP or decoder.

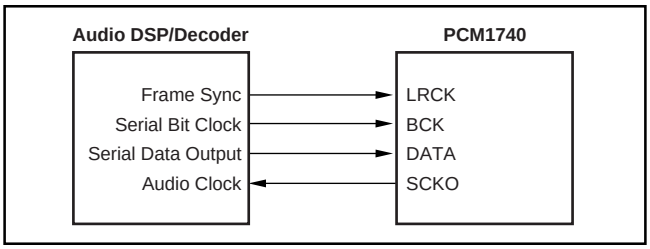


FIGURE 8. Interfacing the PCM1740 to an Audio DSP.

LRCK and BCK Rates

The LRCK input is operated at the sampling frequency, f_S. The BCK input is operated at 32, 48, or 64 times the sampling frequency. Both LRCK and BCK must be synchronous with the SCKO output for proper operation.

Data Formats

The PCM1740 supports two audio interface formats: Standard and I²S. These formats are shown in Figure 9. The audio data word length for the Left and Right channels may be 16-, 20-, or 24-bits. The audio data word length and format are programmed using Control Registers 2 and 3. The reset default condition is Standard format with 16-bit audio data.

Timing Requirements

Figure 10 shows the audio interface timing requirements.

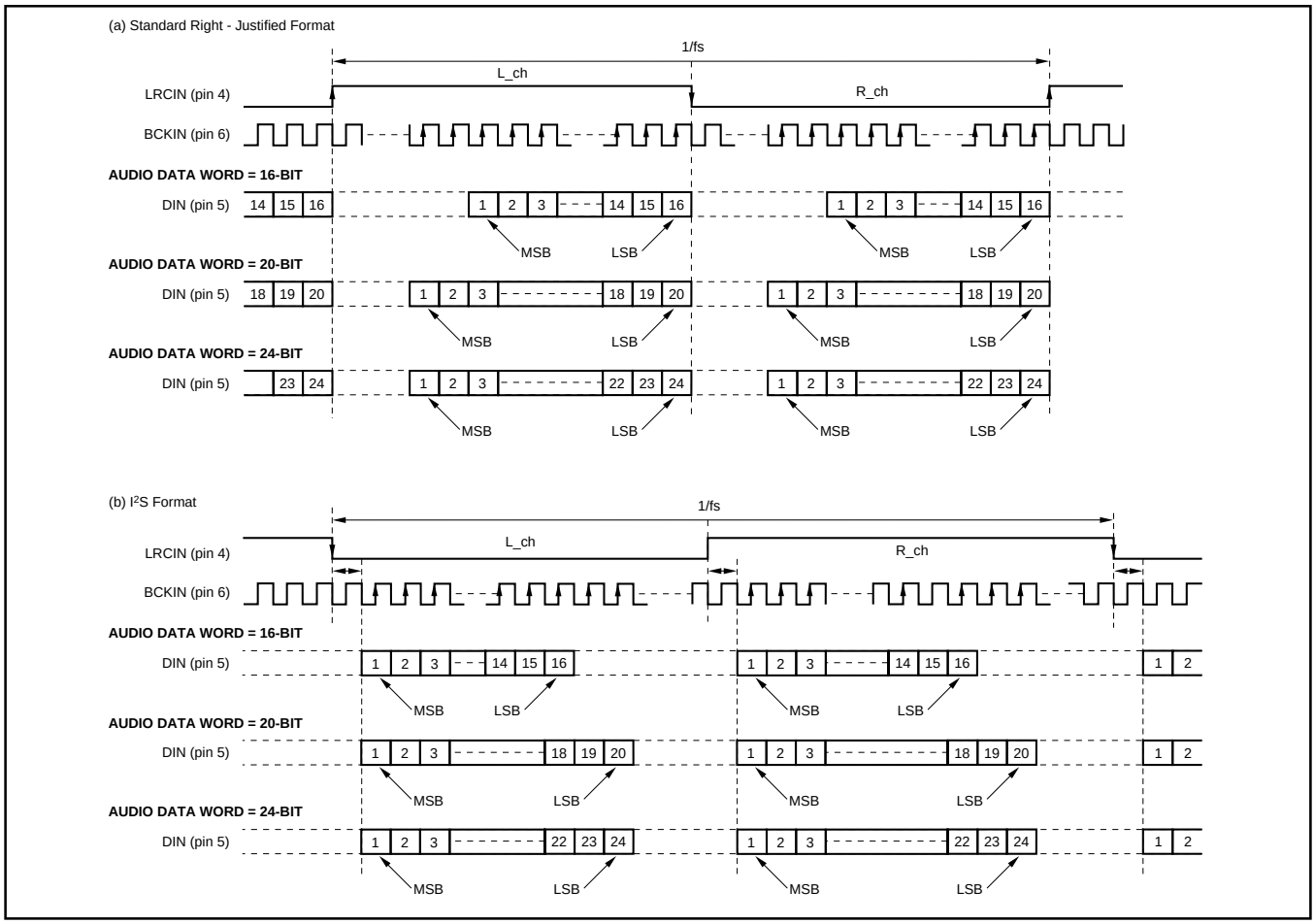
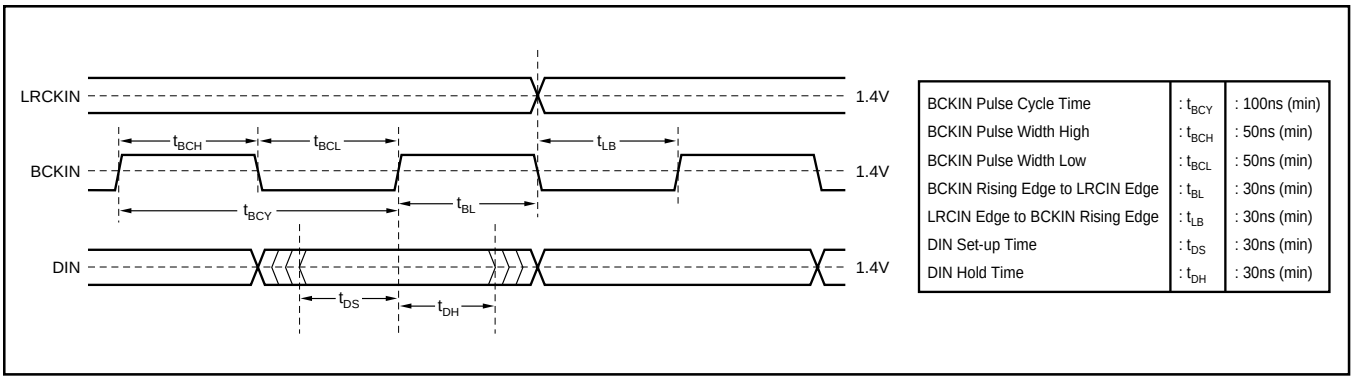


FIGURE 9. Audio Interface Formats.



BCKIN Pulse Cycle Time	: t_{BCY}	: 100ns (min)
BCKIN Pulse Width High	: t_{BCH}	: 50ns (min)
BCKIN Pulse Width Low	: t_{BCL}	: 50ns (min)
BCKIN Rising Edge to LRCIN Edge	: t_{BL}	: 30ns (min)
LRCIN Edge to BCKIN Rising Edge	: t_{LB}	: 30ns (min)
DIN Set-up Time	: t_{DS}	: 30ns (min)
DIN Hold Time	: t_{DH}	: 30ns (min)

FIGURE 10. Audio Interface Timing.

Loss of Synchronization

Ideally, LRCK and BCK will be derived from the SCKO output, ensuring synchronous operation. For other cases, the PCM1740 includes circuitry to detect loss of synchronization between the LRCK and the system clock, SCKO. A loss of synchronization condition is detected when the phase relationship between SCKO and LRCK exceeds ±6 BCK cycles during one sample period, or $1/f_S$. If a loss of synchronization condition is detected, the DAC operation will halt within one sample period and the analog outputs will be forced to $V_{CC}/2$ until re-synchronization between LRCK and SCKO is completed. Figure 11 shows the state of the analog outputs given a loss of synchronization event. During the undefined states, as well as transitions between normal and undefined states, the analog outputs may generate audible noise.

USER PROGRAMMABLE FUNCTIONS

The PCM1740 includes a number of programmable functions, which are configured using five control registers. These registers are accessed using the I^2C-Bus interface.

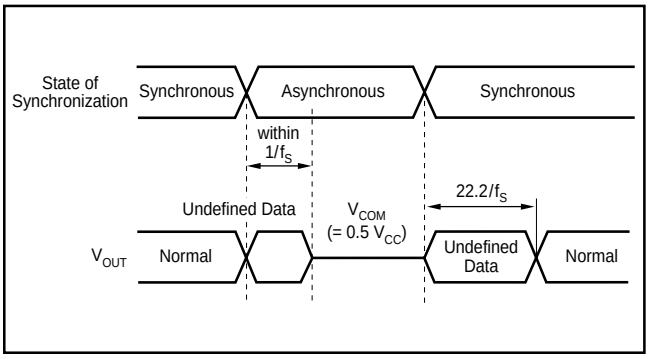


FIGURE 11. Loss of Synchronization and Analog Output State.

This section describes the control registers, while the I^2C-Bus interface is described in a later section. Table II lists the available functions and their corresponding reset default condition.

Register Map

The control register map is shown in Table III. Sub-address bits B8 through B10 are used to specify the register that is being written. All reserved bits, shown as “res”, must be set to ‘0’.

Register Descriptions

The following pages provide detailed descriptions of the five control registers and their associated functions. All reserved bits, shown as “res”, must be set to ‘0’.

FUNCTION	MODE BY DEFAULT
Audio Data Format Select: Standard Format / I^2S Format	Standard Format
Audio Data Word Select: 16-Bit / 20-Bit / 24-Bit	16-Bit
Polarity of LR-clock Selection	Left/Right = HIGH/LOW
De-emphasis Control: OFF, 32kHz, 44.1kHz, 48kHz	OFF
Soft Mute Control	OFF
Attenuation Data for Left-channel	0dB
Attenuation Data for Right-channel	0dB
Attenuation Data Mode Control	Left-channel, Right-channel Individually
Analog Output Mode Select	Stereo Mode
Infinity Zero Detect Mute Control	OFF
DACs Operation Control	ON
System Clock Select: $256f_S/384f_S$	$384f_S$
Sampling Frequency Select: 32kHz Group, 44.1kHz Group, 48kHz Group	44.1kHz Group
Sampling Frequency Multiplier: Normal/Double/Half	Normal, x1

TABLE II. User-Programmable Functions.

	SUB ADDRESS BYTE								DATA BYTE							
REGISTER	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 0	res	res	res	res	res	A2	A1	A0	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0
Register 1	res	res	res	res	res	A2	A1	A0	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
Register 2	res	res	res	res	res	A2	A1	A0	PL3	PL2	PL1	PL0	IW1	IW0	DEM	MUT
Register 3	res	res	res	res	res	A2	A1	A0	SF1	SF0	DSR1	DSR0	SYS	ATC	LRP	IIS
Register 4	res	res	res	res	res	A2	A1	A0	res	res	res	res	res	OPE	IZD	LD

TABLE III. Control Register Map.

REGISTER DEFINITIONS

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 0	res	res	res	res	res	0	0	0	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0

Left Channel Attenuation Data

Default: AL[7:0] = FF_{HEX}

Register 0 is used to set the digital attenuation level for the Left Channel. If the ATC bit in Register 3 is set to '1', then these data are also used to control the Right Channel attenuation. The attenuation level is defined by the following relationships:

Attenuation (dB) = 20 x log ($AL[7:0]_{DEC}$ ÷ 256), when AL[7:0] = 01_{HEX} (1_{DEC}) through FE_{HEX} (254_{DEC})
Attenuation (dB) = –∞ (or Mute), when AL[7:0] = 00_{HEX}
Attenuation (dB) = 0dB, when AL[7:0] = FF_{HEX}

The Attenuation Load bit, LD, in Register 4 must be set to '1' in order to update attenuation settings.
If LD is set to '0', the attenuation remains at the previously programmed level, ignoring the new data until LD is set to '1'.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 1	res	res	res	res	res	0	0	1	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0

Right Channel Attenuation Data

Default: AR[7:0] = FF_{HEX}

Register 1 is used to set the digital attenuation level for the Right Channel. If the ATC bit in Register 3 is set to '1', then the Left Channel attenuation data in Register 1 are used to control the Right Channel attenuation. The attenuation level is defined by the following relationships:

Attenuation (dB) = 20 x log ($AR[7:0]_{DEC}$ ÷ 256), when AR[7:0] = 01_{HEX} (1_{DEC}) through FE_{HEX} (254_{DEC})
Attenuation (dB) = –∞ (or Mute), when AR[7:0] = 00_{HEX}
Attenuation (dB) = 0dB, when AR[7:0] = FF_{HEX}

The Attenuation Load bit, LD, in Register 4 must be set to '1' in order to update attenuation settings.
If LD is set to '0', the attenuation remains at the previously programmed level, ignoring the new data until LD is set to '1'.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 2	res	res	res	res	res	0	1	0	PL3	PL2	PL1	PL0	IW1	IW0	DEM	MUT

MUT **Soft Mute Control**

The MUT bit controls the soft mute function. Soft mute changes the digital attenuation level for both the Left and Right channels, stepping from the currently programmed value to infinite attenuation one step per sample period, or $1/f_S$. This provides a quiet muting of the outputs without audible noise.

MUT = 0	Soft Mute Disabled (default)
MUT = 1	Soft Mute Enabled

DEM **Digital De-Emphasis**

The DEM bit controls the digital de-emphasis function, which is valid only for 32kHz, 44.1kHz, and 48kHz sampling frequencies. The de-emphasis plots are shown in the *Typical Characteristics* section of this data sheet.

DEM = 0	De-Emphasis OFF (default)
DEM = 1	De-Emphasis ON

IW0 **Audio Data Word Length**

IW1

The IW0 and IW1 bits are used to select the data word length for the audio serial interface. The audio data format is selected using the IIS bit in Register 3.

IW1	IW0	Word Length
0	0	16-bits (default)
0	1	20-bits
1	0	24-bits
1	1	Reserved

PL[3:0] **Analog Output Mode Select**

Bits PL[3:0] are used to set the output mode for the analog outputs. Refer to the table below.

PL3	PL2	PL1	PL0	$V_{OUT}L$	$V_{OUT}R$	Notes
0	0	0	0	Mute	Mute	Mute
0	0	0	1	Left	Mute	
0	0	1	0	Right	Mute	
0	0	1	1	(L+R)/2	Mute	
0	1	0	0	Mute	Left	
0	1	0	1	Left	Left	
0	1	1	0	Right	Left	Reverse
0	1	1	1	(L+R)/2	Left	
1	0	0	0	Mute	Right	
1	0	0	1	Left	Right	Stereo (default)
1	0	1	0	Right	Right	
1	0	1	1	(L+R)/2	Right	
1	1	0	0	Mute	(L+R)/2	
1	1	0	1	Left	(L+R)/2	
1	1	1	0	Right	(L+R)/2	
1	1	1	1	(L+R)/2	(L+R)/2	Mono

Register 3

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	0	1	1	SF1	SF0	DSR1	DSR0	SYS	ATC	LRP	IIS

IIS **Audio Data Format**

The IIS bit is used to select the audio data format, either Standard Right-Justified or I^2S.

IIS = 0	Standard Right Justified (default)
IIS = 1	I^2S

LRP **LRCK Polarity**

The LRP bit selects the polarity of left/right clock input (LRCK) when using the Standard Right-Justified audio data format. This bit has no effect when using the I^2S audio data format.

LRP = 0	Left Channel when LRCK = High; Right Channel when LRCK = Low (default)
LRP = 1	Left Channel when LRCK = Low; Right Channel when LRCK = High

ATC **Attenuation Mode Control**

The ATC bit is used to select independent or common attenuation data for the Left and Right channels.

ATC = 0	Independent: Left Channel uses Register 0 and Right Channel uses Register 1 (default)
ATC = 1	Common: Left and Right Channels both use Register 0

SYS **Audio System Clock (or SCKO)**

The SYS bit is used to select the system clock (or SCKO) frequency, either $256f_S$ or $384f_S$.

SYS = 0	$384f_S$ (default)
SYS = 1	$256f_S$

DSR0 **Sampling Frequency Multiplier**

DSR1

The DSR0 and DSR1 bits are used to select the multiplier used in conjunction with the SF0 and SF1 bits.

DSR1	DSR0	Multiplier
0	0	Normal, x1 (default)
0	1	Double, x2
1	0	Half, x 1/2
1	1	Reserved

SF0 **Sampling Frequency Select**

SF1

The SF0 and SF1 bits are used to select the sampling frequency group (32kHz, 44.1kHz, or 48kHz). Frequency selection must be made with an interval time greater than 20µs. The DSR0 and DSR1 bits, described previously, are used to select the multiplier.

SF1	SF0	Sampling Frequency Group
0	0	44.1kHz Group (22.05kHz, 44.1kHz, or 88.2kHz) (default)
0	1	48 kHz Group (24kHz, 48kHz, or 96kHz)
1	0	32 kHz Group (16kHz, 32kHz, or 64kHz)
1	1	Reserved

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 4	res	res	res	res	res	1	0	0	res	res	res	res	res	OPE	IZD	LD

LD **Attenuation Data Load Control**

The LD bit is used to simultaneously set the Left and Right digital attenuation data. When LD is set to '1', the digital attenuation data given by Registers 0 and 1 are loaded for the Left and Right channels. When LD is set to '0', updates to Registers 0 and 1 are ignored, and the attenuation settings remain as previously programmed until LD is set to '1'.

LD = 0	Disabled
LD = 1	Enabled: Left and Right Attenuation Data Updated Simultaneously

IZD **Infinite Zero Detect Mute**

The IZD bit is used to enable/disable the infinite zero detect mute function. The PCM1740 includes infinite zero detection logic that monitors the audio data at the DATA input (pin 18). If the audio data for both the Left and Right channels are all zeros for 65,536 continuous BCK clock cycles, the zero flag will be activated and output amplifier will be disconnected from the output of the delta-sigma modulator. The output amplifier input is switched to the DC common-mode voltage. This forces $V_{OUT}L$ and $V_{OUT}R$ to $V_{CC}/2$. The $\overline{ZERO}$ output flag (pin 16) is not affected by the setting of this bit.

IZD = 0	Disabled (default)
IZD = 1	Enabled

OPE **DAC Operation Control**

The OPE bit is used to enable/disable the operation of the DACs. When enabled, the DAC outputs are connected to the output amplifier for normal operation. When disabled, the output amplifier is disconnected from the DAC output and switched to the DC common-mode voltage. This forces $V_{OUT}L$ and $V_{OUT}R$ to $V_{CC}/2$.

OPE = 0	Enabled: Normal Operation(default)
OPE = 1	Disabled: Outputs forced to $V_{CC}/2$

I²C-BUS INTERFACE DESCRIPTION

The PCM1740 includes an I²C-Bus interface for writing the internal control registers. This provides an industry standard method for interfacing a host CPU control port to the PCM1740. The PCM1740 operates as a Slave receiver on the bus, and supports data transfer rates up to 100 kilobits-per-second (kbps).

The I²C-Bus interface is comprised of four signals: SDA (pin 9), SCL (pin 8), AD0 (pin 6), and AD1 (pin 7). The SCL input is the serial data clock, while SDA is the serial data input. SDA carries start/stop, slave address, sub-address (or register address), register, and acknowledgment data. The AD0 and AD1 inputs form the lower two bits of the slave address.

Slave Address

The PCM1740 Slave address consists of seven bits, as shown in Figure 12. The five most significant bits are fixed, while the two least significant bits, named A0 and A1, are defined by the logic levels present at the AD0 and AD1 input pins. This allows four PCM1740s to reside on the same I²C-Bus.

Bus Operation

Figure 13 shows the typical configuration of the PCM1740 on the I²C-Bus. The Master transmitter or transmitter/receiver is typically a microcontroller, or an audio DSP/decoder. The Master device controls the data transfers on the bus. The PCM1740 operates as a Slave receiver, and accepts data from the Master when it is properly addressed. The data transfer may be comprised of an unlimited number of bytes, or 8-bit data words. Figure 14 shows the message transfer protocol.

For normal bit transfer on the bus, data on SDA must be static while SCL is High. Data on SDA may change High/Low states when SCL is Low. The exception to this rule is the Start and Stop conditions.

The Start condition is defined by a High-to-Low transition on SDA while SCL is High, and is denoted with an 'S' in Figure 12. The Stop condition is defined by a Low-to-High transition on SDA while SCL is High, and is denoted with a 'P' in Figure 12. The Start and Stop conditions are always generated by the Master. All data transfers from Master to Slave begin with a Start condition and end with a Stop condition. The bus is considered to be busy after the Start condition, and becomes free some time after the Stop condition.

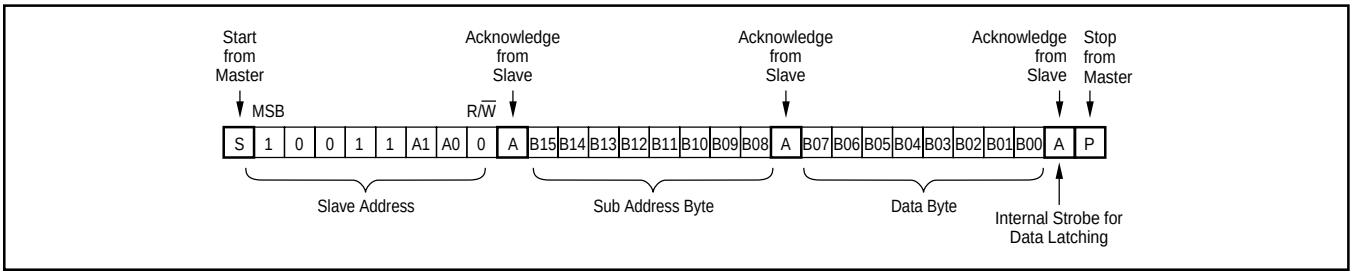


FIGURE 12. Control Data Format.

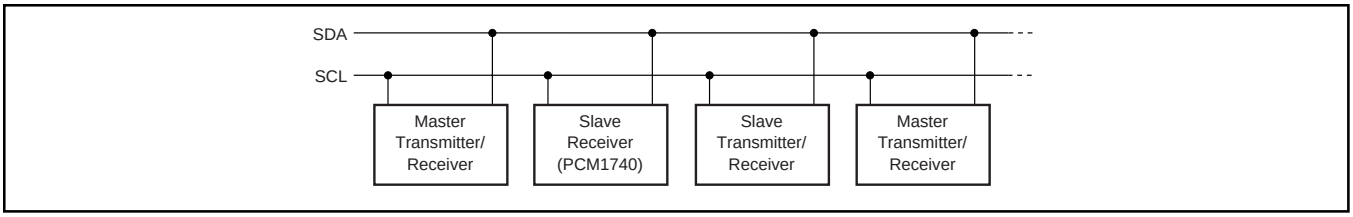
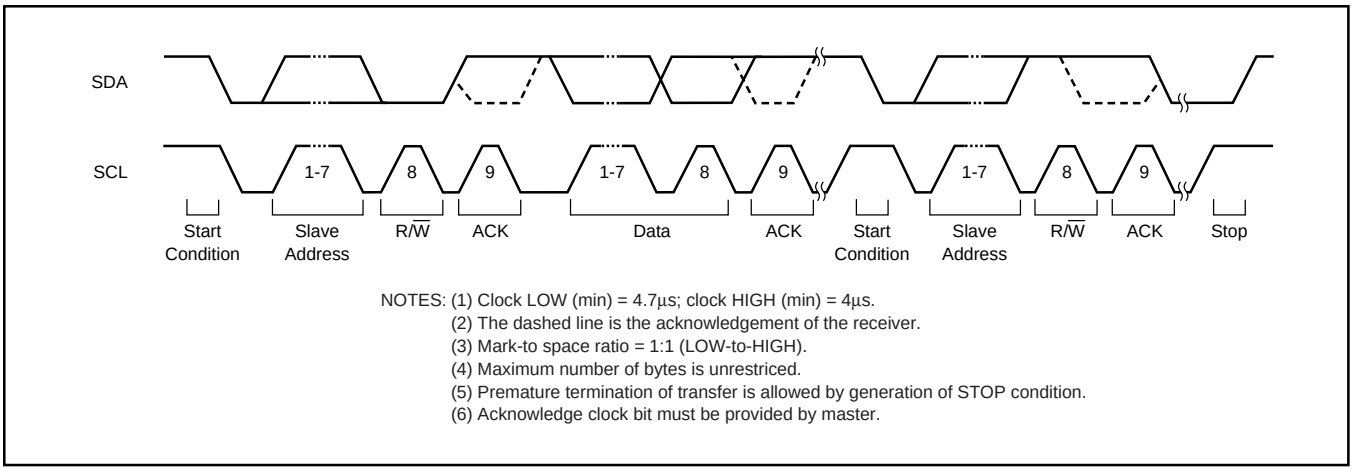


FIGURE 13. Typical I²C-Bus Configuration.



NOTES: (1) Clock LOW (min) = 4.7µs; clock HIGH (min) = 4µs.
(2) The dashed line is the acknowledgement of the receiver.
(3) Mark-to space ratio = 1:1 (LOW-to-HIGH).
(4) Maximum number of bytes is unrestriced.
(5) Premature termination of transfer is allowed by generation of STOP condition.
(6) Acknowledge clock bit must be provided by master.

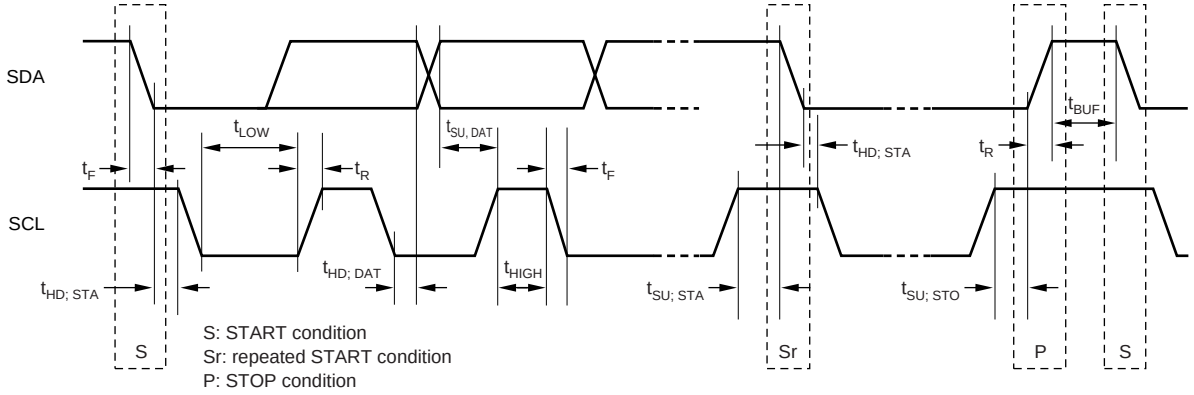
FIGURE 14. I²C Bus Data Transfer.

Data transfer begins with a Start condition, and is immediately followed by the Slave address and Read/Write bit. The Read/Write bit is set to '0' for the PCM1740, in order to write data to the control register specified by the sub-address. This is followed by an acknowledgment from the PCM1740, the sub-address (that is, the control register address), another acknowledgment from the PCM1740, the control register data, and another acknowledgment from the PCM1740. What happens after this depends on if the user wants to continue writing additional control registers, or if they want to terminate the data transfer. If the user wants to continue, the acknowledgment is followed by a Start condition for the next write sequence. If the user decides to terminate the data transfer, then a Stop condition is generated by the Master.

The I^2C-Bus specification defines timing requirements for devices connected to the bus. Timing requirements for the PCM1740 are shown in Figure 15.

Reference

For additional information regarding the I^2C-Bus, please refer to the I^2C-Bus Specification available online from NXP Semiconductors.



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
f_{SCL}	SCL Clock Frequency			100	kHz
$t_{HD; STA}$	Hold time (repeated) START condition, after this period, the first clock pulse is generated	4.0			µs
t_{LOW}	LOW period of the SCL clock	4.7			µs
t_{HIGH}	HIGH period of the SCL clock	4.0			µs
$t_{SU:STA}$	Set-up time for a repeated START condition	4.7			µs
$t_{HD;DAT}$	Data hold time for I^2C-BUS devices	0		3.45(2)	µs
$t_{SU;DAT}$	Data set-up time	250			ns
t_R	Rise time of both SDA and SCL signals			1000	ns
t_F	Fall time of both SDA and SCL signals			300	ns
$t_{SU;STO}$	Set-up time for STOP condition	4.0			µs
t_{BUF}	Bus free time between a STOP and START condition	4.7			µs
C_B	Capacitive load for each bus line			400	pF
V_{NL}	Noise margin at the LOW level for each connected device (including hysteresis)	0.1 V_{DD}			V
V_{NH}	Noise margin at the HIGH level for each connected device (including hysteresis)	0.2 V_{DD}			V

FIGURE 15. I^2C Bus Timing.

APPLICATIONS INFORMATION

BASIC CONNECTION DIAGRAM

A basic connection diagram is shown in Figure 16. Power supply and reference decoupling capacitors should be located as close as possible to the PCM1740 package. The 27MHz crystal should also be located as close as possible to the package, to reduce the effects of parasitic capacitance on VCXO operation.

A single +5V supply is recommended, to avoid issues with power-supply sequencing and SCR latch-up. It is recommended that this supply be separate from the system digital power supply. In cases where this is not practical, an inductor or ferrite bead should be placed in series with the +5V supply connection to reduce or eliminate high-frequency noise on the supply line.

In cases where overshoot or ringing is present on the LRCK or BCK signals, a series resistance of 25Ω to 100Ω should be added. The resistor forms a simple RC filter with the device input and printed circuit board (PCB) parasitic capacitance, dampening the overshoot and ringing effects, while reducing high-frequency noise emissions.

TYPICAL APPLICATION DIAGRAM

Figure 17 shows the PCM1740 being used as part of the audio sub-system in a set-top box application.

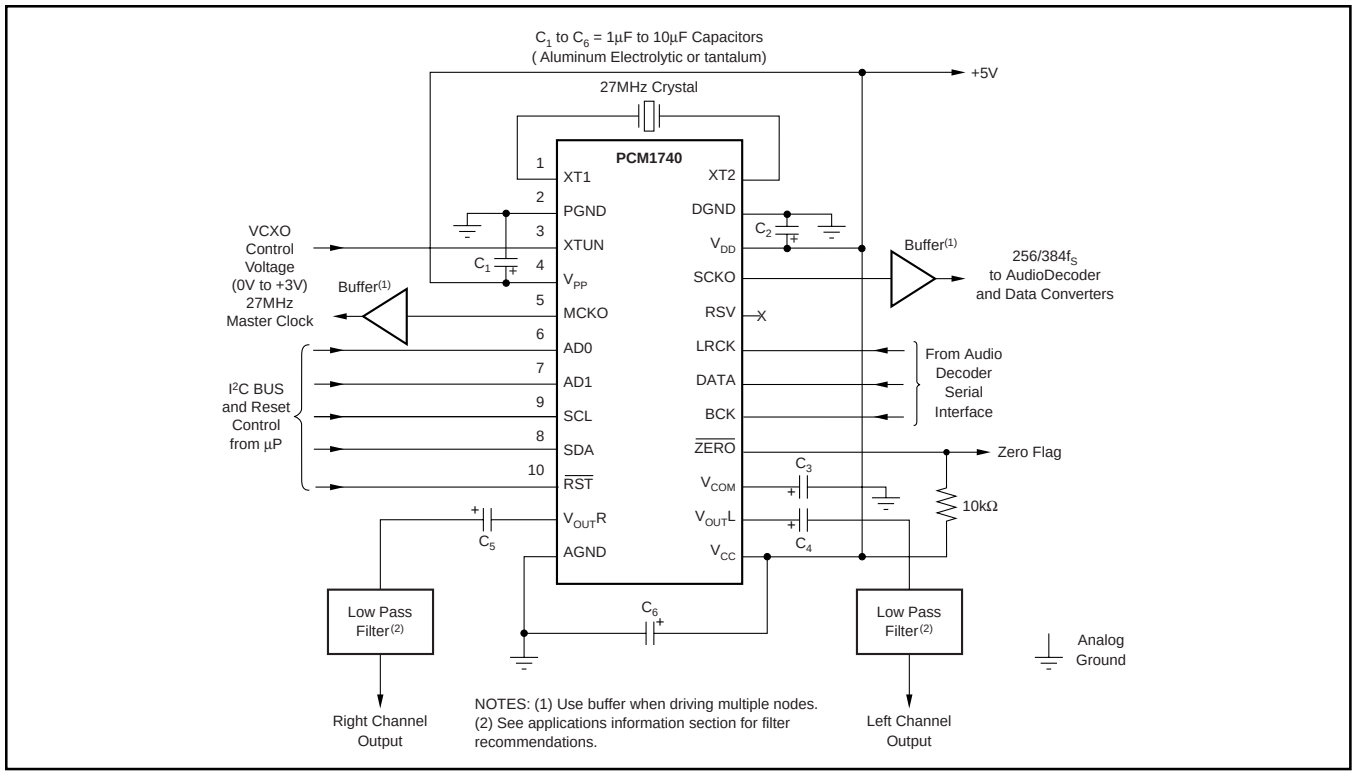


FIGURE 16. Basic Connection Diagram.

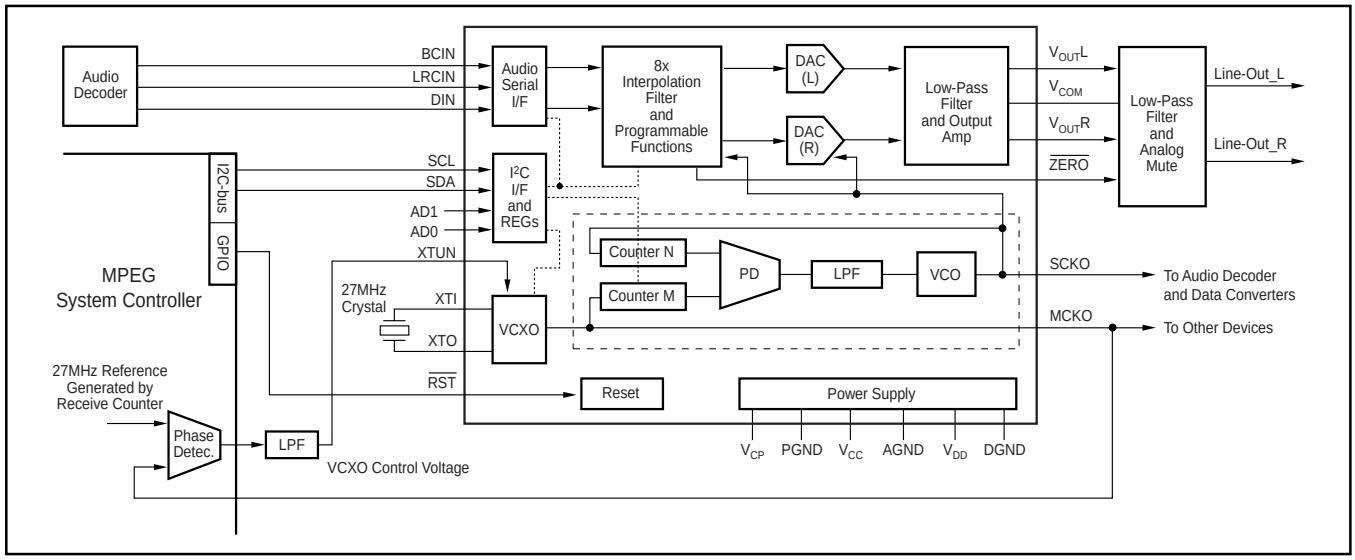


FIGURE 17. Typical Application Diagram.

The VTUN control voltage is generated by the MPEG-2 controller, which compares the MCKO output clock from the PCM1740 with the clock count received from the transmitter. VTUN is adjusted to retain clock synchronization between the transmitted and received signals. The SCKO output is used as the audio master clock for the audio decoder and additional data converters.

V_{COM} Output

The unbuffered DC common-mode voltage output, V_{COM} (pin 15), is brought out mainly for de-coupling purposes. V_{COM} is nominally biased to $V_{CC}/2$. The V_{COM} output may be used to bias external circuits, but it must be connected to a high-impedance node or buffered using a voltage follower. Figure 18 shows examples of the proper use of the V_{COM} output for external biasing applications.

DAC OUTPUT FILTERING

Delta-Sigma DACs utilize noise shaping techniques to improve in-band signal-to-noise (SNR) performance at the expense of generating increased out of band noise above the Nyquist frequency, or $f_S/2$. The out-of-band noise must be low-pass filtered in order to provide optimal converter performance. This is accomplished by a combination of on-chip and external low-pass filtering.

The PCM1740 includes an on-chip low-pass filter as part of the output amplifier stage. The frequency response for the filter is shown in the *Typical Characteristics* section of this data sheet. The –3dB cutoff frequency is fixed at 100kHz.

Figure 19 shows the recommended external low-pass active filter circuits for dual and single-supply applications. These circuits are second-order Butterworth filters using the Multiple Feedback (MFB) circuit arrangement. Both filters have a cutoff frequency of 30kHz. Figure 19(a) is a dual-supply filter with a gain of 1.85 (for a standard 2 V_{RMS} line output level). Figure 19(b) is a single-supply filter with a gain of 1. Values for the filter components may be calculated using the FilterPro program, available from the TI web site (www.ti.com) and local sales offices. For more information regarding MFB active filter design and the FilterPro program, refer to TI Application Report SBFA001.

Since the overall system performance is defined primarily by the quality of the DACs and their associated analog output circuitry, op amps designed specifically for audio applications are recommended for the active filters. TI's OPA2134, OPA2353, and OPA2343 dual op amps are ideal for use with the PCM1740.

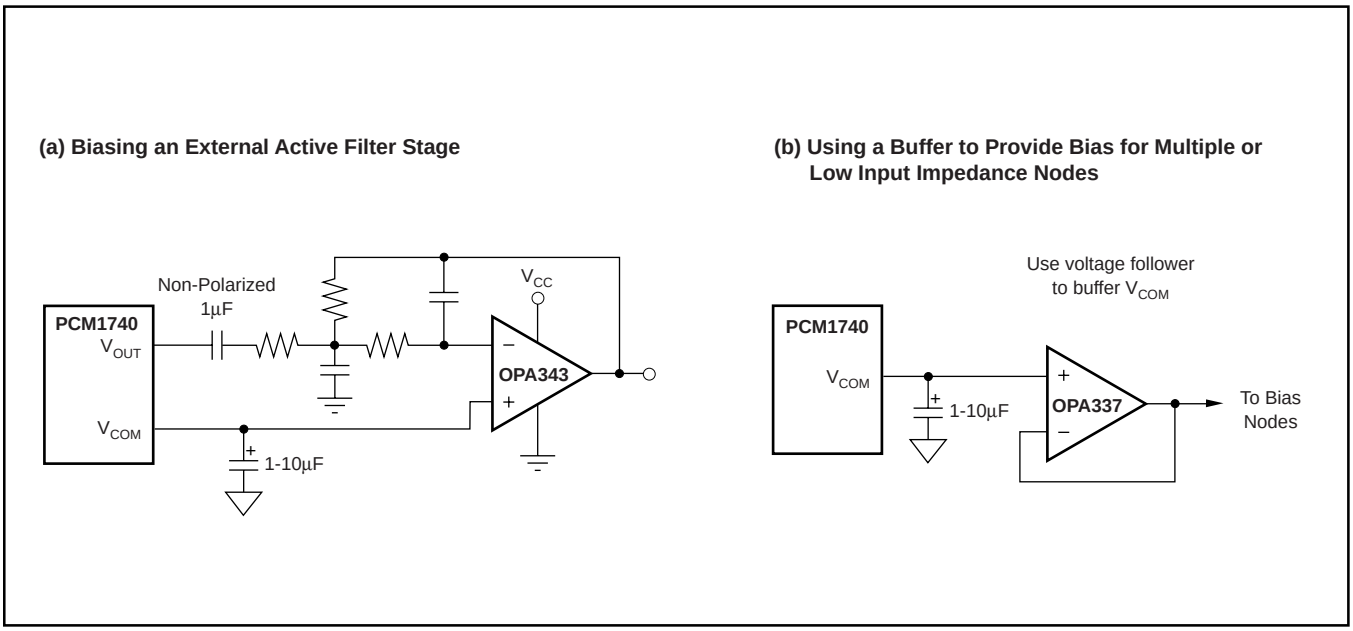


FIGURE 18. Using V_{COM} To Bias External Circuitry.

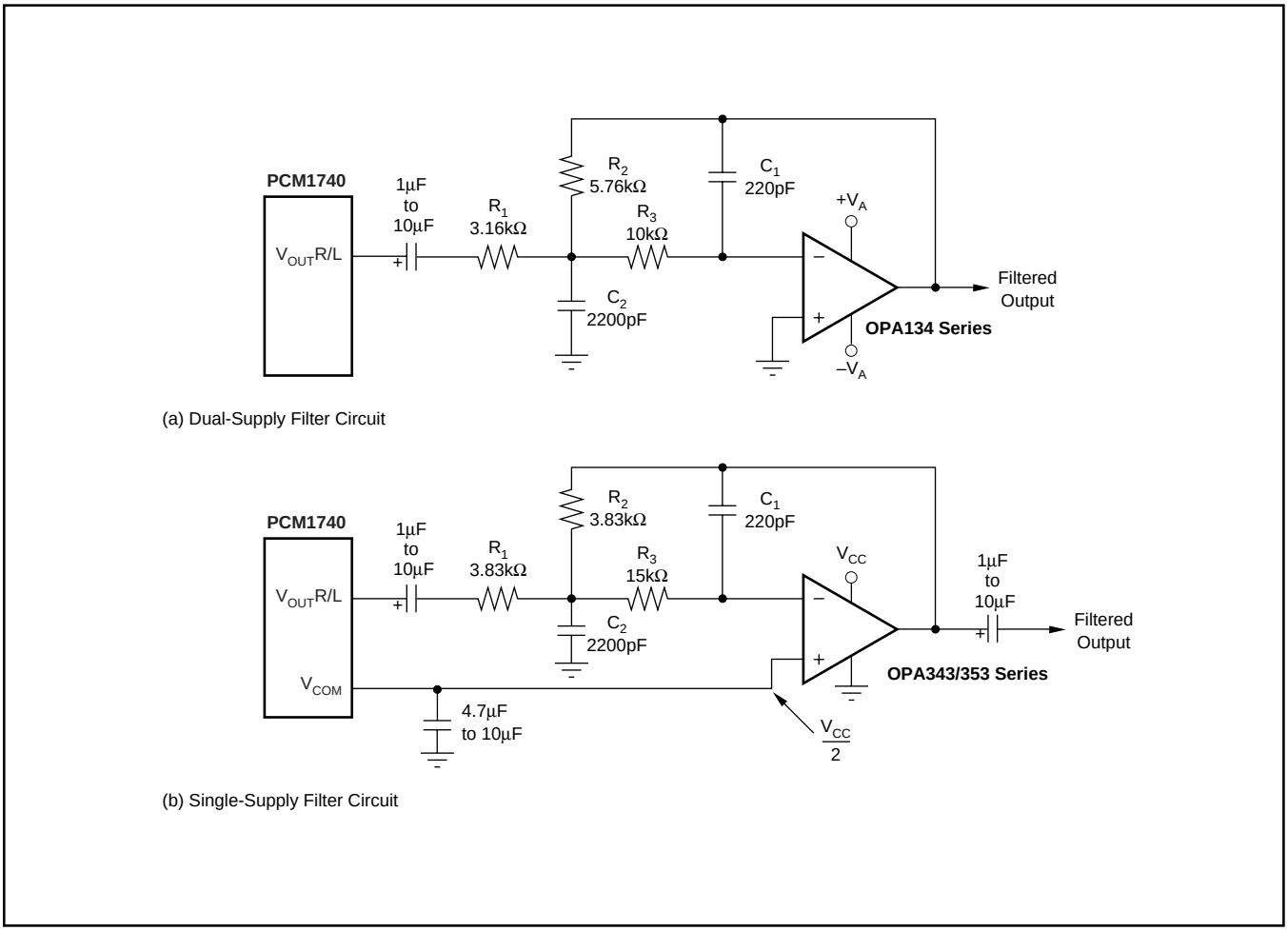


FIGURE 19. Recommended Output Filter Circuits.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
5/07	B	—	Entire Document	Updated format.
		2	Electrical Characteristics	Changed Low Level Output Voltage V_{OH} to V_{OL} (typo)
		14	SF0, SF1	Added sentence regarding interval time must be greater than 20µs.
		15	Figure 12	Changed Figure 12.
			Figure 14	Changed Figure 14.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM1740E	ACTIVE	SSOP	DB	24	58	RoHS & Green	Call TI	Call TI		PCM1740E	Samples
PCM1740E/2K	ACTIVE	SSOP	DB	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		PCM1740E	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

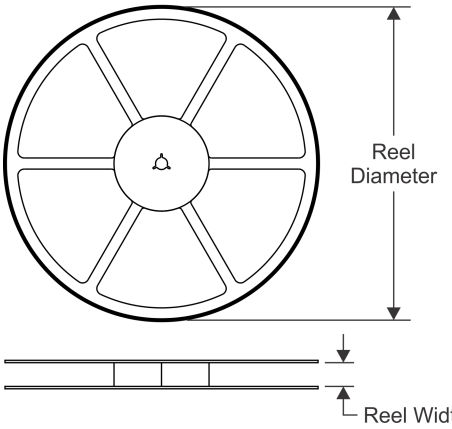
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

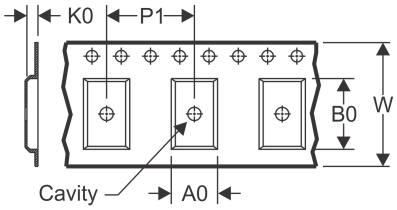
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

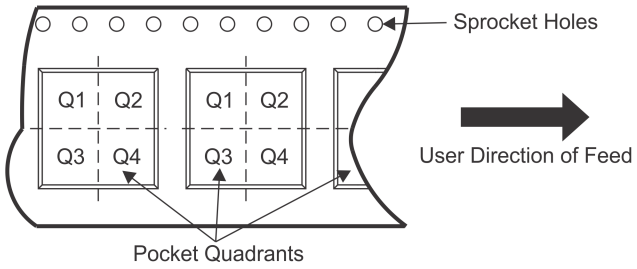


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

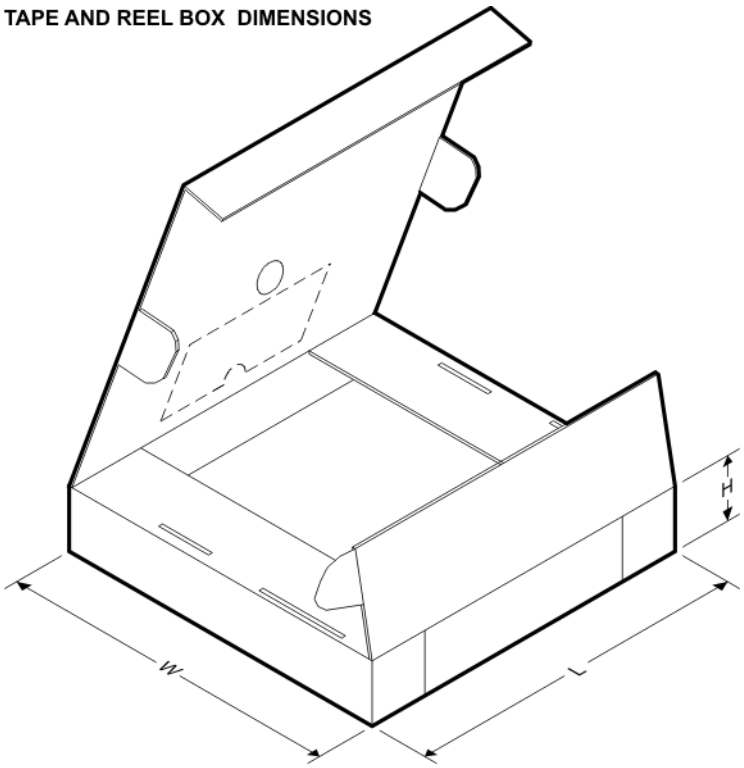
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM1740E/2K	SSOP	DB	24	2000	330.0	17.4	8.5	8.6	2.4	12.0	16.0	Q1

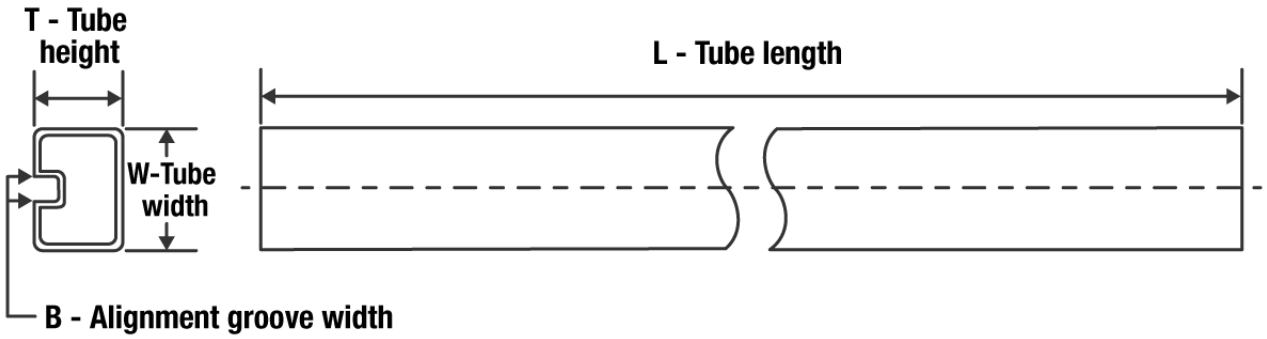
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM1740E/2K	SSOP	DB	24	2000	336.6	336.6	28.6

TUBE



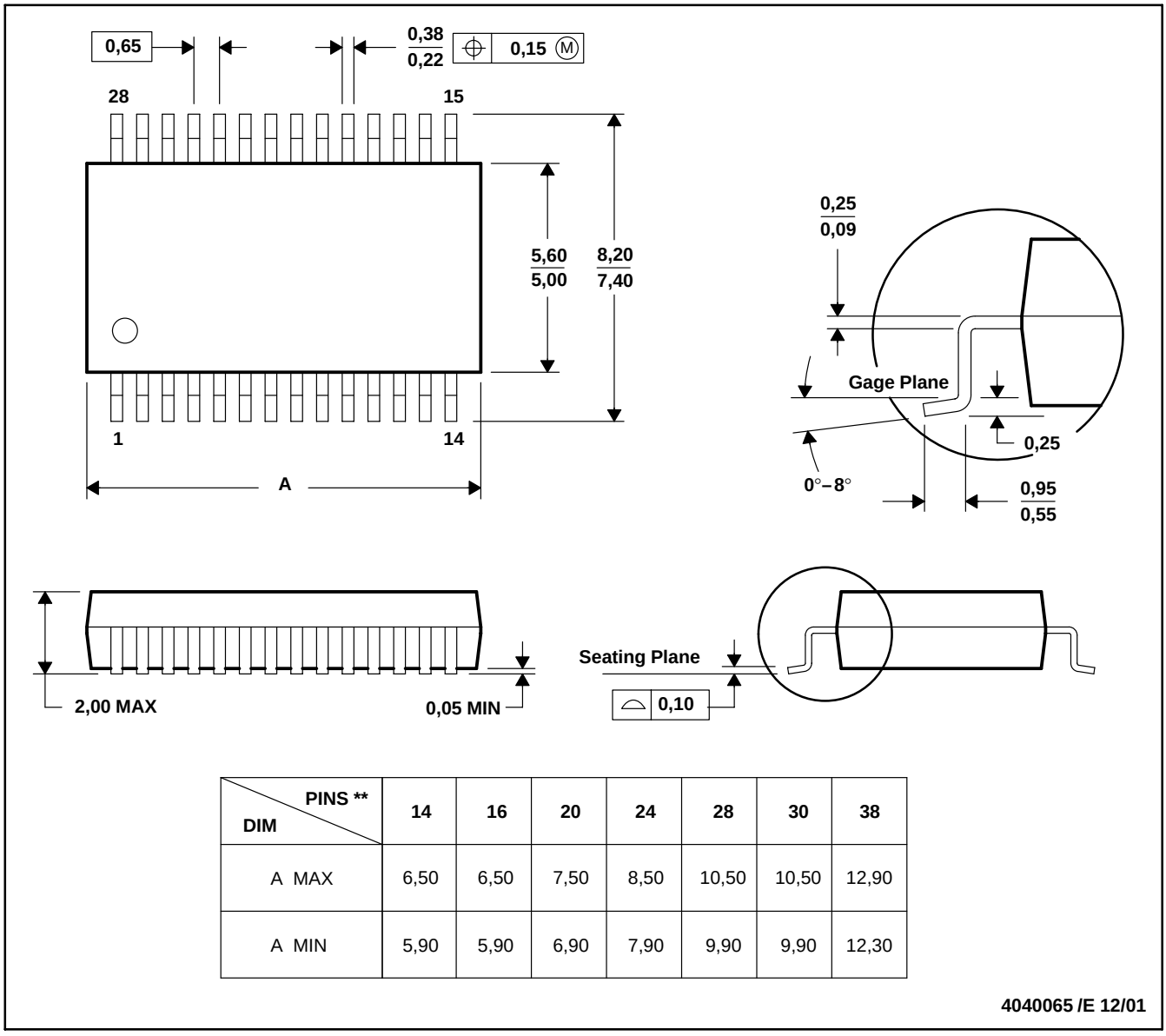
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
PCM1740E	DB	SSOP	24	58	500	10.6	500	9.6

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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