Final Product Change Notification

202105041F01 : S12ZVC/A/19/12/64/96 FAB SITE EXPANSION (NXP-ATMC to TSMC10)

Note: This notice is NXP Company Proprietary.

Issue Date: Jun 09, 2021 **Effective date:** Sep 07, 2021

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Change Category

[ ]Wafer Fab Process	[ ]Assembly Process	[ ]Product Marking	[ ]Test Process	[ ]Design
[ ]Wafer Fab Materials	[ ]Assembly Materials	[ ]Mechanical Specification	[ ]Test Equipment	[X]Errata
[X]Wafer Fab Location	[ ]Assembly Location	[ ]Packing/Shipping/Labeling	[ ]Test Location	[ ]Electrical Spec/Test Coverage
[ ]Firmware	[X]Other: Reference Manual and Errata updated to include TSMC10 mask set information.			

PCN Overview

Description

NXP Semiconductors is announcing the introduction of Taiwan Semiconductor Manufacturing Company Fab 10 (TSMC10), Shanghai, China as a dual source wafer manufacturing location for the S912ZVC/A/19/12/64/96.

NXP Semiconductors requires the use of Flex part numbers to maximize supply continuity. Without the use of Flex part numbers, backlog will have to be converted from one fab sourced device to another fab sourced device as capacity dictates.

The Data Sheet & Reference Manual for S912ZVC/A/19/12/64/96 has been updated by adding the TSMC10 mask set (0P81C & 1P81C) in section 1.6.1 Part ID Assignments and the Part Ordering Information's mask set identifier suffix
"S12ZVC_0N23N, Mask Set Errata for Mask 0N23N" have been updated to cover both N23N and P81C mask sets. Errata e8188: ADC: High current in Stop Mode was also revised in the updated document.

The S912ZVC/A/19/12/64/96 Data Sheet, Reference Manual and Errata is attached with this notification or can be found at: https://www.nxp.com/products/processors-and-microcontrollers/additional-mpu-mcus-architectures/s12-magniv-mixed-signal-mcus/s12zvc-mixed-signal-mcu-for-automotive-industrial-can-applications:S12ZVC?tab=Documentation_Tab

Corresponding ZVEI Delta Qualification Matrix ID: SEM-DS-02, SEM-PW-08, SEM-PW-13

Reason

The Fab manufacturing site capacity expansion to TSMC10 will improve NXP's ability to meet increasing customer demand and still maintain supply from the original Fab (NXP-ATMC).

Identification of Affected Products

Top Side Marking
The mask marking for TSMC10 will reflect P81C, while the mask marking for ATMC will remain N23N.

Product Availability

Sample Information:
Samples are available from Jun 25, 2021
Production
Planned first shipment Sep 13, 2021

Anticipated Impact on Form, Fit, Function, Reliability or Quality

No Impact on form, fit, function, reliability or quality
Data Sheet Revision
A new datasheet will be issued
Disposition of Old Products
Fab Expansion. No depletion of inventory required.

Timing and Logistics

In compliance with JEDEC J-STD-046, your acknowledgement of this change is expected by Jul 09, 2021.

Contact and Support

For all inquiries regarding the ePCN tool application or access issues, please contact NXP "Global Quality Support Team".

For all Quality Notification content inquiries, please contact your local NXP Sales Support team.

At NXP Semiconductors we are constantly striving to improve our product and processes to ensure they reach the highest possible Quality Standards. Customer Focus, Passion to Win.

NXP Quality Management Team.

About NXP Semiconductors

NXP Semiconductors N.V. (NASDAQ: NXPI) provides High Performance Mixed Signal and Standard Product solutions that leverage its leading RF, Analog, Power Management, Interface, Security and Digital Processing expertise. These innovations are used in a wide range of automotive, identification, wireless infrastructure, lighting, industrial, mobile, consumer and computing applications.

NXP Semiconductors

High Tech Campus, 5656 AG Eindhoven, The Netherlands

Affected OPN	12NC
S912ZVC12F0MKH	935322402557
S912ZVC12F0MKHR	935322402528
S912ZVC12F0MLF	935312538557
S912ZVC12F0MLFR	935312538528
S912ZVC12F0VKH	935320591557
S912ZVC12F0VKHR	935320591528
S912ZVC12F0VLF	935320618557
S912ZVC12F0VLFR	935320618528
S912ZVC19F0MKH	935315208557
S912ZVC19F0MKHR	935315208528
S912ZVC19F0MLF	935318326557
S912ZVC19F0MLFR	935318326528
S912ZVC19F0VKH	935312621557
S912ZVC19F0VKHR	935312621528
S912ZVC19F0VLF	935320842557
S912ZVC19F0VLFR	935320842528
S912ZVC19F1WLF	935399646557
S912ZVC19F1WLFR	935399646528
S912ZVC64F0CLF	935333108557
S912ZVC64F0CLFR	935333108528
S912ZVC64F0MKH	935315885557
S912ZVC64F0MKHR	935315885528
S912ZVC64F0MLF	935316231557
S912ZVC64F0MLFR	935316231528
S912ZVC64F0VLF	935324979557
S912ZVC64F0VLFR	935324979528
S912ZVC96F0CLF	935377439557
S912ZVC96F0MKH	935324998557
S912ZVC96F0MKHR	935324998528
S912ZVC96F0MLF	935312973557
S912ZVC96F0MLFR	935312973528
S912ZVC96F0VLF	935386068557
S912ZVC96F0VLFR	935386068528
S912ZVCA19F0MKH	935317743557
S912ZVCA19F0MLF	935313152557
S912ZVCA19F0MLFR	935313152528
S912ZVCA19F0VLF	935322502557
S912ZVCA19F0VLFR	935322502528
S912ZVCA19F0WKH	935312421557
S912ZVCA19F1WLF	935399606557
S912ZVCA19F1WLFR	935399606528
S912ZVCA64F0CLF	935333111557
S912ZVCA64F0CLFR	935333111528
S912ZVCA64F0MLF	935325024557
S912ZVCA64F0MLFR	935325024528
S912ZVCA64F0VLF	935375244557
S912ZVCA64F0VLFR	935375244528
S912ZVCA64F0WKH	935323896557
S912ZVCA96F0MLF	935316267557
S912ZVCA96F0MLFR	935316267528
S912ZVCA96F0VLF	935316485557
S912ZVC12F1MLF	935422804557
S912ZVC19F1MKH	935428303557
S912ZVC12F1MLFR	935422804528
S912ZVCA19F1WKH	935422334557
S912ZVCA96F0MKH	935420419557
S912ZVCA96F0MKHR	935420419528

S12ZVC/A/19/12/64/96 (HEARST)
ATMC VS TSMC10 CAPACITY EXPANSION

AUTOMOTIVE PROCESSORS
28-MAY-2021

EXTERNAL USE

SECURE CONNECTIONS FOR A SMARTER WORLD

180nm UHV Wafer Capacity Expansion

- Consistent with NXP's previous communications and in alignment with our policy of providing flexible sourcing and supply assurance, NXP qualified Carcassonne in Q4 2020 and has now completed qualification for Hearst (all 180nm UHV wafer technology) at Taiwan Semiconductor Manufacturing Company Fab 10 (TSMC10), Shanghai, China.

- NXP requires the use of Flex part numbers to maximize supply continuity and provide best possible lead time. Without the use of Flex part numbers, backlog will have to be converted from one fab sourced device to another fab sourced device as capacity dictates.

- Carcassonne is the first MagniV product to be dual qualified, ATMC / TSMC10 in Q4 2020.

- Knox128 and Tomar3 have successfully completed dual qualification, ATMC / TSMC10 in Q1 2021.

- Knox32 have successfully completed dual qualification, ATMC / TSMC10 in Q2 2021.

TSMC10 Overview

- *High volume, 200mm fab F10-TSMC located in Shanghai, China*
  - *Fab Area: 24,000m*
  - *Low defectivity, high volume Accumulative 10M Wafer Out*
  - *Monthly capacity 130K wfr/month*
  - *follows the same quality system as tsmc cooperate HQ*
- *Production Status*
  - *>50 customers, >250 products, >1 million accumulated wafers*
- *Comprehensive Solution 0.5um~0.11um technology*
  - *3.3V or 5V I/O*
  - *High endurance or low leakage devices*
- *Automotive grade certified*
  - *Grade1 18HDR since 2014*
  - *ISO/IATF16949 since 2017*
    - *13 technology. Qualified on Grade 1; 23 products from 7 customers*
- *NXP-Fab10 business engagement*

Summary of Changes

Process Step	Changes	Details
Wafer Fab	• **TSMC10 becomes a dual wafer source**	• **Process electrical characteristics matched** • **No Data Sheet specification changes**
Design	• **No Design changes**	• **No Design changes**
Packaging	• **Packages qualified with same Build of Material**	• **No difference in product performance**
Marking	• **Mask # is marked on product so that customers can** visually distinguish ATMC or TSMC10.	• **Slide #5 & #6 provides marking details**
Test	• **No Change to Test Flow, Specification or Quality**	• **No difference in product performance** • **Electrical Distributions (ED) comparison, ATMC vs TSMC, included in PCN**
Reliability	• **Passed AECQ100 qualification**	**Qualification Report available within PCN**
Orderable Part Numbers	• ***Required conversion to "Flex" part number for supply assurance.***	• ***Slide #5 & #6 provides part number details***

Changes within the AEC Q100 Certification of Design, Construction and Qualification (CofDC)

Supplier Name: NXP Semiconductors	Date: 10Jan2018	Date: 18March2021
Item Name	**Supplier Response**	**Supplier Response**
1. User's Part Number:	See PPAP	See PPAP
2. Supplier's Part Number/Data Sheet:	S9S12ZVC/A/19/12/64/96FxxLF/KH S9S12ZVC/A/19/12/64/96FxxLF/KH	S9S12ZVC/A/19/12/64/96AxxLF/KH S9S12ZVC/A/19/12/64/96AxxLF/KH
3. Device Description:	LL18UHV	LL18UHV
4. Wafer/Die Fab Facility & Process ID:		
a. Facility name/plant #:	NXP-ATMC	TSMC10
b. Street address:	3501 Ed Bluestein Boulevard; Austin, TX 78721 (ATMC)	4000, Wen Xiang Road, Songjiang, Shanghai, Postcode: 201616
c. Country:	USA	China
8. Wafer/Die:		
a. Wafer Size:	200mm	200mm
b. Die family:	SGF180	SGF180
c. Die mask set revision & name:	0N23N, 1N23N	0P81C, 1P81C
d. Die photo:	Available upon request	Available upon request
9. Die Technology Description:		
a. Wafer/Die process technology:	E018	E018
b. Die channel length (µM):	0.18	0.18
c. Die gate length (µM):	0.18	0.18
d. Die supplier process ID (mask #):	N23N	P81C
e. Number of transistors or gates:	Gates: 643609	Gates: 643609
f. Number of mask steps:	37	37
10. Die Dimensions:		
a. Die width (mm):	3.85	3.85
b. Die length (mm):	3.5	3.5
c. Die thickness (finished) (mm):	0.28	0.28
11. Die Metallization:		
a. Die metallization materials:	Al(0.5%Cu)	Al(0.5 wt%Cu)
b. Number of layers:	5	5
c. Thickness (per layer):	4KA (M1~M4), 8KA(LM)	M1~4: 4 kA, M5: 8kA
d. % of alloys (if present):	Al/Cu 0.5%	99.5% Al/0.5% Cu
12. Die Passivation:		
a. Number of passivation layers:	3	3
b. Die passivation material(s):	HDP Oxide+SRON+PEN	10kA HDP + 1.5kA PE-OX + 6kA PE-SN
c. Thickness (es) & tolerances:	10K HDP+1.5KSRON+6KPEN(+/-6.5%)	P1. HDPOX-10KA: target:10000A, SPEC +/-1000A P2. Oxide-1.5K: target:1500A, SPEC:+/-150A P3. SiN-6K: target: 6000A, SPEC: +/-700A

S12ZVC/A/19/12/64/96 (Hearst) Order Part Numbers and Marking

Required

ATMC PNs	TSMC10 PNs	Flex PNs	
S912ZVC/A ff F0 t pp / R	S912ZVC/A ff L0 t pp / R	S912ZVC/A ff A t pp / R	ff = Flash memory size 12 = 128Kb; 64 = 64Kb; 19 = 192Kb; 96 = 96Kb t = Temp range (W, M, V, C): min -40C to W = 150C, M = 125C, V = 105C, C = 85C pp = package; LF = 48LQFP; KH = 64LQFP-EP
F0 = ATMC 0 = Rev 0	L0 = TSMC10 0 = Rev 0	(No wafer fab designator) A = ATMC /TSMC10 Rev0	

Marking		ATMC	TSMC10	
Line 1	Logo			
Line 2	Base Part No.	S912ZVC/A ff t pp		
Line 3	Mask#	0N23N	0P81C	
Line 4	Trace code	ALYWZ		A =Assembly site L =Lot ID Y =Year; W=week Z =Sub lot

S12ZVC/A/19/12/64/96 (Hearst) Order Part Numbers and Marking

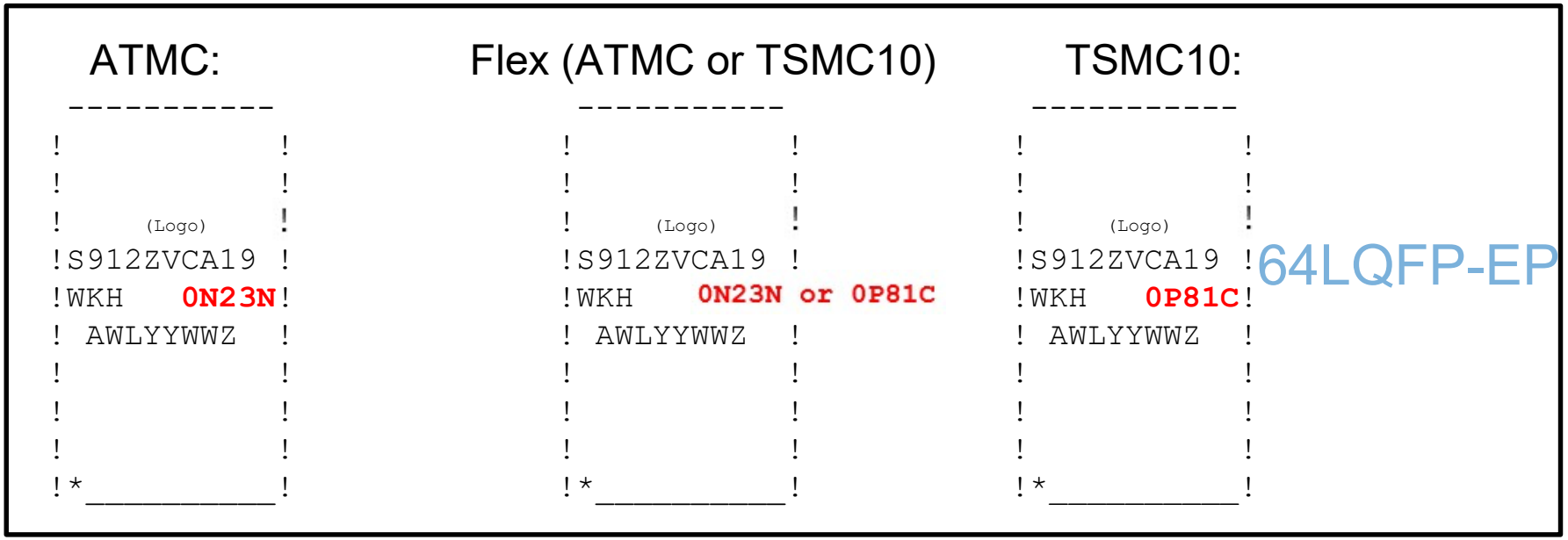
Required

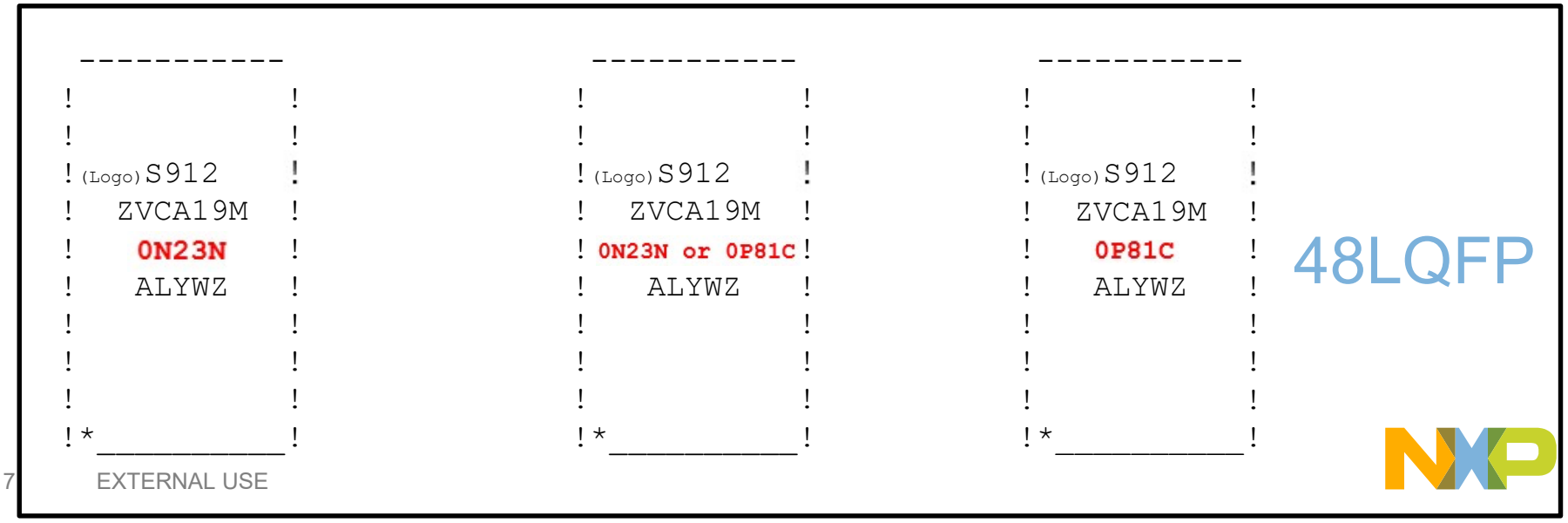
ATMC PNs	TSMC10 PNs	Flex PNs	
S912ZVC/A ff F1 t pp / R	S912ZVC/A ff L1 t pp / R	S912ZVC/A ff A1 t pp / R	ff = Flash memory size 12 = 128Kb; 64 = 64Kb; 19 = 192Kb; 96 = 96Kb t = Temp range (W, M, V, C): min -40C to W = 150C, M = 125C, V = 105C, C = 85C pp = package; LF = 48LQFP; KH = 64LQFP-EP
F1 = ATMC 1= Rev 1	L1 = TSMC10 1 = Rev 1	(No wafer fab designator) A1 = ATMC /TSMC10 Rev1	

Marking		ATMC	TSMC10	
Line 1	Logo			
Line 2	Base Part No.	S912ZVC/A ff t pp		
Line 3	Mask#	1N23N	1P81C	
Line 4	Trace code	ALYWZ		A =Assembly site L =Lot ID Y =Year; W=week Z =Sub lot

S12ZVC/A/19/12/64/96 (Hearst) Order Part Numbers and Marking

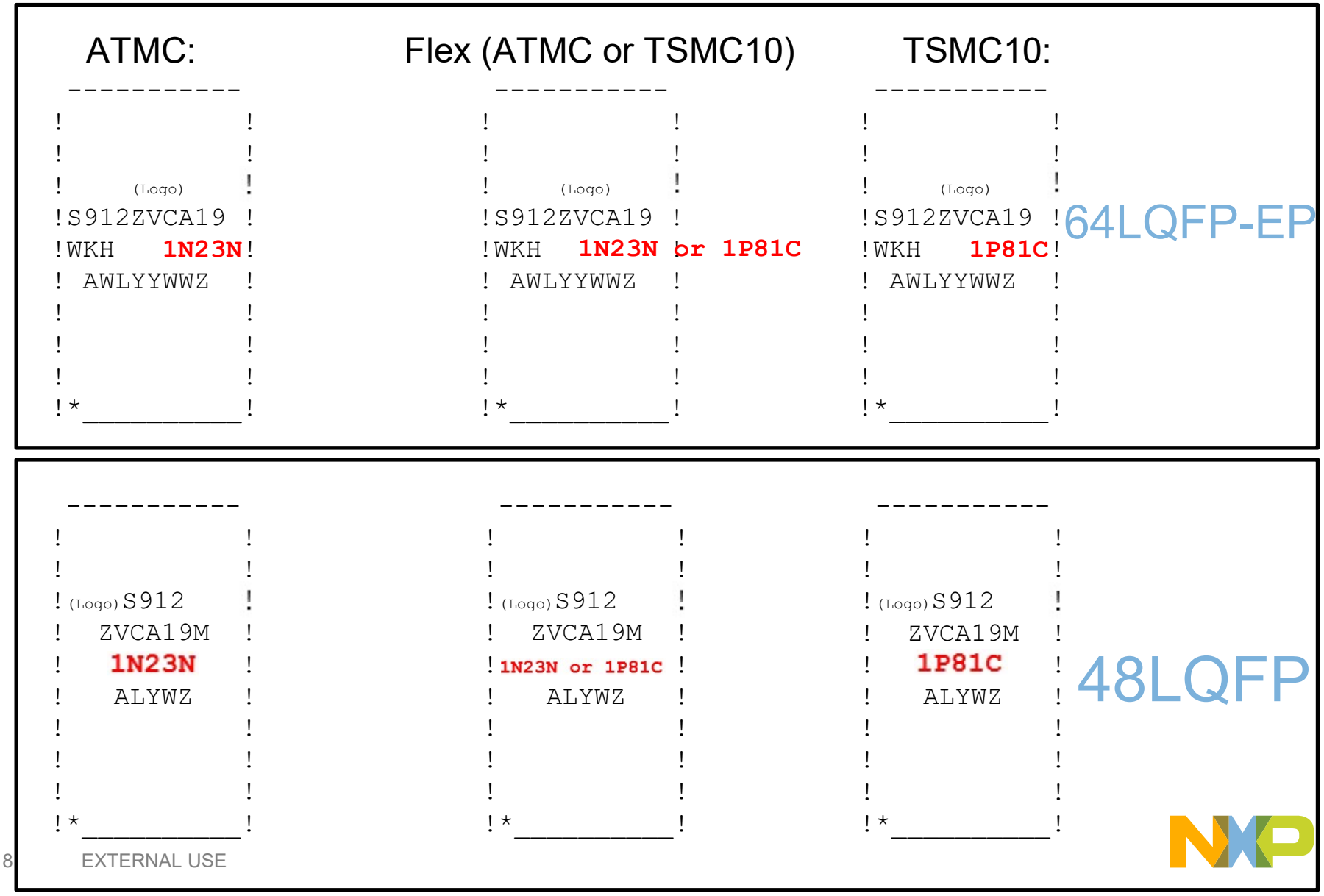
- ***How to distinguish between the ATMC and TSMC10 marking?***





S12ZVC/A/19/12/64/96 (Hearst) Order Part Numbers and Marking

- ***How to distinguish between the ATMC and TSMC10 marking?***



TSMC10 Part ID

Device	Mask Set Number	Part ID
MC9S12ZVCA64	0N23N	05.1D.10.00
	0P81C	
	1N23N	05.1D.10.01
	1P81C	
MC9S12ZVCA96	0N23N	05.1D.10.00
	0P81C	
	1N23N	05.1D.10.01
	1P81C	
MC9S12ZVCA128	0N23N	05.1D.10.00
	0P81C	
	1N23N	05.1D.10.01
	1P81C	
MC9S12ZVCA192	0N23N	05.1D.10.00
	0P81C	
	1N23N	05.1D.10.01
	1P81C	
MC9S12ZVC64	0N23N	05.1D.10.00
	0P81C	
	1N23N	05.1D.10.01
	1P81C	
MC9S12ZVC96	0N23N	05.1D.10.00
	0P81C	
	1N23N	05.1D.10.01
	1P81C	
MC9S12ZVC128	0N23N	05.1D.10.00
	0P81C	
	1N23N	05.1D.10.01
	1P81C	
MC9S12ZVC192	0N23N	05.1D.10.00
	0P81C	
	1N23N	05.1D.10.01
	1P81C	

TSMC10 mask set Part ID used the same with ATMC N23N.

No other register difference between two Fabs.

TSMC10 mask set P81C will be included in the updated Data Sheet.

S12ZVC/A/19/12/64/96 (Hearst) TSMC10 Expansion - Table below provides sample part numbers:

ATMC Part #	TSMC10 Qualified Sample Part #	Package
S912ZVC19F0MLF	K912ZVC19L0MLF	48LQFP
S912ZVC19F0VLF	K912ZVC19L0VLF	48LQFP
S912ZVC19F0VLFR	K912ZVC19L0VLFR	48LQFP
S912ZVC64F0VLFR	K912ZVC64L0VLFR	48LQFP
S912ZVC96F0MLFR	K912ZVC96L0MLFR	48LQFP
S912ZVC19F1WLFR	K912ZVC19L1WLFR	48LQFP
S912ZVCA19F1WLFR	K912ZVCA19L1WLFR	48LQFP

For custom part number samples, please check with your NXP representative for availability.

AEC-Q100H Qual Results

Objective:	**S912ZVC12 Hearst Grade0 TSMC10 Fab Site Expansion Qualification**				
NXP PN: S912ZVCA19L0WKH Part Name: Hearst	Customer Name(s): Varies PN(s):			Plan or Results: See below revision Revision # & Date:	
Technology: LL18UHV Package: LQFP-EP 64 10*10*1.4 P.5 LQFP 48 7*7*1.4P0.5	Designer Not Applicable			QUARTZ Tracking #: 263449 (0P81C) - 64LQFP-EP 263798 (1P81C) - 64LQFP-EP 263452 (0P81C) - 48LQFP 263799 (1P81C) - 48LQFP	
Fab / Assembly / Final Test Sites: TSMC10 / NXP-ATTJ / NXP-ATTJ	Product Engr: Tom Zhang				(Signature/Date shown below may be electronic)
Maskset#: P81C Rev#: 0 & 1	Prod. Package Engr: WH Chan			PPE Approval (for DIM/BOM results) WH Chan Signature & Date: 25-May-2021	
Die Size (in mm) 3.500 X 3.850 W x L	NPI PRQE: Chew Kim Seong			NPI PRQE Approval Signature & Date: Chew Kim Seong 25-May-2021	
Part Operating Temp. Grade: Grade 0 –40°C to 150°C	Trace/DateCode:	Lot A 8EME00HM4T00 (0P81C) 64LQFP-EP	--- --- ---	CAB Approval 20090424B Signature & Date: 4-June-2021	
		Lot B 8EME00HPPR00 (1P81C) 64LQFP-EP	Lot C 8EME00HPPS00 (1P81C) 64LQFP-EP	Lot D 8EME00HPPT00 (1P81C) 64LQFP-EP	Customer Approval May be N/A Signature & Date:
		Lot E 8EME00HM5H (0P81C) 48LQFP	Lot F 8EME00HSWC00 (1P81C) 48LQFP	---	

TESTS HIGHLIGHTED IN YELLOW ARE PERFORMED FOR THIS STUDY

This testing is performed by NXP Reliability Lab (ATTJ) unless otherwise noted in the Comments.

GROUP A - ACCELERATED ENVIRONMENTAL STRESS TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments or Generic Data
PC	JESD22-A113 J-STD-020	**Preconditioning (PC) :** PC required for SMDs only. MSL 3 @ 260°C, +5/-0°C	TEST @ RH	All surface mount devices prior to HAST, UHST, TC, and as required per test conditions.			Lot A: 0/77 Lot E: 0/77	**Generic Data** S912ZVML64L1AWKH_CCS, (0P58A_TSMC10), 64LQFP-EP 10*10, NXP-ATTJ, Q259405: Lot A: 0 / 231 Lot B: 0 / 231 Lot C: 0/ 231 S912ZVL12_Knox128, (0P59C_TSMC10), 48LQFP 7*7, NXP-ATTJ, Q261895: Lot A: 0/231
HAST	JESD22-A101 A110	**Highly Accelerated Stress Test (HAST):** PC before HAST (for SMDs only): Required HAST = 110°C/85% for 264hrs. Bias = Max Vdd	TEST @ RH	77	0	0	Pass	**Generic Data** S912ZVML64L1AWKH_CCS, (0P58A_TSMC10), 64LQFP-EP 10*10, NXP-ATTJ, Q259405: Lot A: 0 / 77 Lot B: 0 / 77 Lot C: 0/ 77 S912ZVL12_Knox128, (0P59C_TSMC10), 48LQFP 7*7, NXP-ATTJ, Q261895: Lot A: 0 / 77
UHST	JESD22-A102 A118	**Unbiased HAST (UHST):** PC before UHST (for SMDs only): Required UHAST = 110°C/85% for 264hrs.	TEST @ R	77	0	0	Pass	**Generic Data** S912ZVML64L1AWKH_CCS, (0P58A_TSMC10), 64LQFP-EP 10*10, NXP-ATTJ, Q259405: Lot A: 0 / 77 Lot B: 0 / 77 Lot C: 0/ 77 S912ZVL12_Knox128, (0P59C_TSMC10), 48LQFP 7*7, NXP-ATTJ, Q261895: Lot A: 0 / 77
TC	JESD22-A104 AEC Q100-Appendix 3	**Temperature Cycle (TC):** PC before TC (for SMDs only) TC = -55ºC to +150ºC for 2000 cycles For AEC only: WBP after TC on 5 devices from 1 lot; 2 bonds per corner and one mid-bond per side on each device.	TEST @ H For AEC: WBP =/> 3 grams	77	0	0	Pass	**Generic Data** S912ZVML64L1AWKH_CCS, (0P58A_TSMC10), 64LQFP-EP 10*10, NXP-ATTJ, Q259405: Lot A: 0 / 77 WBP: 0/5; minimum > 3.0g Lot B: 0 / 77 Lot C: 0 / 77 S912ZVL12_Knox128, (0P59C_TSMC10), 48LQFP 7*7, NXP-ATTJ, Q261895: Lot A: 0 / 77
HTSL	JESD22-A103	**High Temperature Storage Life (HTSL):** 175°C for 1008hrs.	TEST @ RH	45	0	0	Pass	**Generic Data** S912ZVML64L1AWKH_CCS, (0P58A_TSMC10), 64LQFP-EP 10*10, NXP-ATTJ, Q259405: Lot A: 0 / 45 Lot B: 0 / 45 Lot C: 0 / 45 S912ZVL12_Knox128, (0P59C_TSMC10), 48LQFP 7*7, NXP-ATTJ, Q261895: Lot A: 0 / 45

TEST GROUP B - ACCELERATED LIFETIME SIMULATION TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments or Generic Data
HTOL	JESD22-A108	High Temperature Operating Life: Ta= 150ºC Ta for 1008 hours. Bias = HTOL Vsupply=18V, Core=2.2V and I/O=6V 10k Program Flash W/E Cycling @ 150°C 100K EEPROM W/E Cycling @ 150°C	TEST @ RCH	77	1 (0P81C) 3 (1P81C)	77 231	Lot A: 0/77 (0P81C) Lot B: 0/77 (1P81C) Lot C: 0/77 (1P81C) Lot D: 0/77 (1P81C)	**Generic Data** S912ZVML64L1AWKH_CCS, (0P58A_TSMC10), 64LQFP-EP 10*10, NXP-ATTJ, Q259405: Lot A: 0 / 77 Lot B: 0 / 77 Lot C: 0 / 77 Lot D: 0 / 77 Lot E: 0 / 77 Lot F: 0 / 77 S912ZVL12_Knox128, (0P59C_TSMC10), 48LQFP 7*7, NXP-ATTJ, Q261895: Lot A: 0 / 77 Lot B: 0 / 77 Lot C: 0 / 77
ELFR	AEC Q100-008	Early Life Failure Rate: Ta = 150°C for 48 hrs; Bias = HTOL Vsupply=18V, Core=2.2V and I/O=6V	TEST @ RHC	800	1	800	Lot A: 0/800	**Generic Data** S912ZVML64L1AWKH_CCS, (0P58A_TSMC10), 64LQFP-EP 10*10, NXP-ATTJ, Q259405: Lot A: 0 / 800 Lot B: 0 / 800 Lot C: 0 / 800 S912ZVL12_Knox128, (0P59C_TSMC10), 48LQFP 7*7, NXP-ATTJ, Q261895:Lot A: 0 / 800
EDR	AEC Q100-005	NVM Endurance, Data Retention, 10k Program Flash W/E Cycling @ 150°C 100K EEPROM W/E Cycling @ 150°C DRB@175C for 1008hrs	TEST @ RHC	77	1	77	Lot A: 0/77	**Generic Data** S912ZVML64L1AWKH_CCS, (0P58A_TSMC10), 64LQFP-EP 10*10, NXP-ATTJ, Q259405: Lot A: 0 / 77 Lot B: 0 / 77 Lot C: 0 / 77 S912ZVL12_Knox128, (0P59C_TSMC10), 48LQFP 7*7, NXP-ATTJ, Q261895: Lot A: 0/ 77 Lot B: 0 / 77 Lot C: 0 / 77
EDR	AEC Q100-005	NVM Endurance, Data Retention, 10k Program Flash W/E Cycling @ 25°C 100K EEPROM W/E Cycling @ 25°C DRB@25C for 1008hrs	TEST @ RHC	77	1	77	Lot A: 0/77	**Generic Data** S912ZVML64L1AWKH_CCS, (0P58A_TSMC10), 64LQFP-EP 10*10, NXP-ATTJ, Q259405: Lot A: 0 / 77 Lot B: 0 / 77 Lot C: 0 / 77 S912ZVL12_Knox128, (0P59C_TSMC10), 48LQFP 7*7, NXP-ATTJ, Q261895: Lot A: 0 / 77 Lot B: 0 / 77 Lot C: 0 / 77

TEST GROUP C - PACKAGE ASSEMBLY INTEGRITY TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments or Generic Data
WBS	AEC Q100-001	**Wire Bond shear (WBS)**	Cpk = or > 1.67	30 bonds from minimum 5 units	6	30	64LQFP-EP Lot A: 0/5, Cpk > 1.67 Lot B: 0/5, Cpk > 1.67 Lot C: 0/5, Cpk > 1.67 Lot D: 0/5, Cpk > 1.67 48LQFP Lot E: 0/5, Cpk > 1.67 Lot F: 0/5, Cpk > 1.67	
WBP	MilStd883-2011	**Wire Bond Pull (WBP):** Cond. C or D	Cpk = or > 1.67	30 bonds from minimum 5 units	6	30	64LQFP-EP Lot A: 0/5, Cpk > 1.67 Lot B: 0/5, Cpk > 1.67 Lot C: 0/5, Cpk > 1.67 Lot D: 0/5, Cpk > 1.67 48LQFP Lot E: 0/5, Cpk > 1.67 Lot F: 0/5, Cpk > 1.67	
SD	JESD22-B102	**Solderability (SD):** 8hr.(1 hr. for Au-plated leads) Steam age prior to test. If production burn-in is done, samples must also undergo burn-in prior to SD.	>95% lead coverage of critical areas	15	0	0	Not required	
PD	JESD22-B100	**Physical Dimensions(PD):** PD per NXP drawing	Cpk = or > 1.67	10	0	0	Not required	
DIM & BOM		**Dimensional (DIM):** QAO to verify PD results against valid NXP drawing. **BOM Verification (BOM):** QAO to verify qual lot ERF BOM is accurate.					DIM: Pass BOM: Approve	
SBS	AEC-Q100-010	**Solder Ball Shear (SBS):** Performed on all solder ball mounted packages e.g. PBGA, Chip Scale, Micro Lead Frame (but NOT Flip Chip). Two reflow cycles at MSL reflow temperature before shear.	Cpk = or >1.67	10 (5 balls from a min. of 10 devices)	0	0	Not required	For solder ball mounted packages only; NOT for Flip Chips.
LI	JESD22-B105	**Lead Integrity (LI):** Not required for surface mount devices; Only required for through-hole devices.	No lead breakage or cracks	5 (10 leads from each of 5 parts)	0	0	Not required	

TEST GROUP D - DIE FABRICATION RELIABILITY TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments
EM		**Electro Migration (EM)**						The data, test method, calculations and internal criteria should be available to the customer upon request for new technologies.
TDDB		**Time Dependent Dielectric Breakdown (TDDB)**						The data, test method, calculations and internal criteria should be available to the customer upon request for new technologies.
HCI		**Hot Carrier Injection (HCI)**						The data, test method, calculations and internal criteria should be available to the customer upon request for new technologies.
SM		**Stress Migration (SM)**						The data, test method, calculations and internal criteria should be available to the customer upon request for new technologies.
NBTI		**Negative Bias Temperature Instability (NBTI)**						The data, test method, calculations and internal criteria should be available to the customer upon request for new technologies.

TEST GROUP E - ELECTRICAL VERIFICATION TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments or Generic Data
TEST	NXP Spec	**Pre- and Post Functional / Parametrics (TEST):** For AEC, test software shall meet requirements of AEC-Q100-007. Testing performed to the limits of device specification in temperature and limit value.	0 Fails	All	All	All	Pass	This action refers to Final Testing of all qualification units.
HBM	AEC-Q100-002 / JESD22	**ElectroStatic Discharge/** **Human Body Model Classification (HBM):** **All pins:** Test @ 500/ 1000/ 1500/ 2000 Volts Test @ 4000V for CANH/ CANL/ SPLIT/ HVI pins only. For AEC, see AEC-Q100-002 for classification levels.	TEST @ RH 2KV min.	3 units per Voltage level	1 (0P81C) 1 (1P81C)	15 15	Lot A (0P81C) - 64LQFP-EP 500V: 0/3 (All pins except CANH/ CANL/ SPLIT/ HVI) 1000V: 0/3 (All pins except CANH/ CANL/ SPLIT/ HVI) 1500V: 0/3 (All pins except CANH/ CANL/ SPLIT/ HVI) 2000V: 0/3 (All pins except CANH/ CANL/ SPLIT/ HVI) 4000V: 0/3 (CANH/ CANL/ SPLIT/ HVI pins) Lot B (1P81C) - 64LQFP-EP 500V: 0/3 (All pins except CANH/ CANL/ SPLIT/ HVI) 1000V: 0/3 (All pins except CANH/ CANL/ SPLIT/ HVI) 1500V: 0/3 (All pins except CANH/ CANL/ SPLIT/ HVI) 2000V: 0/3 (All pins except CANH/ CANL/ SPLIT/ HVI) 4000V: 0/3 (CANH/ CANL/ SPLIT/ HVI pins)	
CDM	AEC-Q100-011 or JESD22	**ElectroStatic Discharge/** **Charged Device Model Classification (CDM):** Test @ 250/ 500/ 750(CP) Volts For AEC, see AEC-Q100-011 for classification levels.	TEST @ RH All pins =/> 500V For AEC, Corner pins =/> 750V;	3 units per Voltage level	2 (0P81C) 2 (1P81C)	18 18	Lot A (0P81C) - 64LQFP-EP 250V: 0/3 (all pins) 500V: 0/3 (all pins) 750V: 0/3 (corner pins) Lot B (1P81C) - 64LQFP-EP 250V: 0/3 (all pins) 500V: 0/3 (all pins) 750V: 0/3 (corner pins) Lot E (0P81C) - 48LQFP 250V: 0/3 (all pins) 500V: 0/3 (all pins) 750V: 0/3 (corner pins) Lot F (1P81C) - 48LQFP 250V: 0/3 (all pins) 500V: 0/3 (all pins) 750V: 0/3 (corner pins)	
LU	JESD78 plus AEC-Q100-004 for AEC	**Latch-up (LU):** Test per JEDEC JESD78 with the AEC-Q100-004 requirements for AEC. Ta= 150C operating temperature, +/- 100mA Vsupply = Maximum operating voltage	TEST @ RH	6	1 (0P81C) 1 (1P81C)	6 6	Lot A (0P81C): 0/6 Lot B (1P81C): 0/6	
ED	AEC-Q100-009, NXP spec	**Electrical Distribution (ED)** **T0 and post HTOL**	TEST @ RCH For AEC, Cpk target > 1.67	30	1 (0P81C) 1 (1P81C)	30 30	Lot A (0P81C): 0/30; Cpk>1.67 Lot B (1P81C): 0/30; Cpk>1.67	- Include T0 drift comparison between ATMC and TSMC10. - T0 and post HTOL1008hrs drift comparison.
FG	For AEC, AEC-Q100-007	**Fault Grading (FG)**	FG shall be = or > 90% for qual units				No change	
CHAR	For AEC, AEC-Q003	**Characterization (CHAR):** Ony performed on new technologies and part families per AEC Q003.						
EMC	SAE J1752/3 - Radiated Emissions	**Electromagnetic Compatibility (EMC)** (see AEC Q100 Appendix 5 for test applicability; done on case-by-case basis per customer/NXP agreement)	<40dBuV 150KHz - 1GHz	1	0	0	Not required	

Bill of Material (BOM) of Qualification Device

Quartz#	Fab/Mask Set/Te	Product-Qual Description/Part Number (s)	DIE SIZE(mmxmm)	Assembly Site	Pkg Description/Coo	Mold Description	EPOXY Description	Wire Description
263449 (0P81C) 263798 (1P81C)	TSMC10-FAB/ 0P81C & 1P81C/ LL18UHV	S912ZVC12_Hearst_64LQFP-EP TSMC10 Fab expansion Qual	3.500 x 3.850	NXP-ATTJ	LQFP-EP 64 10*10*1.4 P.5/ 8281	Hitachi CEL- 9240HF16FL	SUMITOMO CRM-1064MBL	25um Cu
263452 (0P81C) 263799 (1P81C)	TSMC10-FAB/ 0P81C & 1P81C/ LL18UHV	S912ZVC12_Hearst_48LQFP TSMC10 Fab expansion Qual	3.500 x 3.850	NXP-ATTJ	LQFP 48 7*7*1.4P0.5 / 6089	Hitachi CEL- 9240HF16FL	SUMITOMO CRM-1064MBL	25um Cu

Package Generic Data List:

Quartz#	Fab/Mask Set/Te	Product-Qual Description/Part Number (s)	DIE SIZE(mmxmm)	Assembly Site	Pkg Description/Coo	Mold Description	EPOXY Description	Wire Description
259405	TSMC10-FAB/ 0P58A/ LL18UHV	S912ZVML12 / S912ZVMC12 TSMC10 Fab expansion Qual	3.52 x 4.37	NXP-ATTJ	LQFP-EP 64 10*10*1.4 P.5/ 8281	Hitachi CEL- 9240HF16FL	SUMITOMO CRM-1064MBL	25um Cu
261895	TSMC10- FAB/0P59C/LL18 UHV	S912ZVL12_Knox128 Grade0 TSMC10 Fab Site Expansion Qualification	3.00 x 3.20	NXP-ATTJ	LQFP 48 7*7*1.4P0.5 / 6089	Hitachi CEL- 9240HF16FL	SUMITOMO CRM-1064MBL	25um Cu

Die Generic Data List:

Quartz#	Fab/Mask Set/Te	Product-Qual Description/Part Number (s)	DIE SIZE(mmxmm)	Assembly Site	Pkg Description/Coo	Mold Description	EPOXY Description	Wire Description
259405	TSMC10-FAB/ 0P58A/ LL18UHV	S912ZVML12 / S912ZVMC12 TSMC10 Fab expansion Qual	3.52 x 4.37	NXP-ATTJ	LQFP-EP 64 10*10*1.4 P.5/ 8281	Hitachi CEL- 9240HF16FL	SUMITOMO CRM-1064MBL	25um Cu
261895	TSMC10-FAB/ 0P59C/ LL18UHV	S912ZVL12_Knox128 Grade0 TSMC10 Fab Site Expansion Qualification	3.00 x 3.20	NXP-ATTJ	LQFP 48 7*7*1.4P0.5 / 6089	Hitachi CEL- 9240HF16FL	SUMITOMO CRM-1064MBL	25um Cu

Revision	Date	Comments	Author
Rev O	25-May-2021	Qualification result update.	Chew Kim Seong

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