Protected LED Array Driver

FEATURES AND BENEFITS

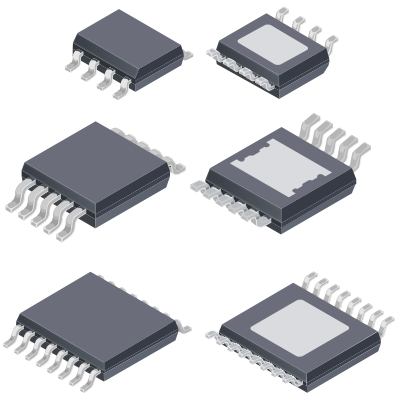
- AEC-Q100 qualified
- Total LED drive current up to 400 mA (LP, LJ, and LY packages) or 300 mA (LJ)
- Current shared equally up to 100 mA by up to 4 strings (LP and LY)
- 6 to 50 V supply
- Low dropout voltage
- LED output short-to-ground and thermal protection
- Disable on open LED detection option
- Enable input for PWM control
- Current slew rate limit during PWM
- Current set by reference resistor
- Automotive temperature range (K, –40°C to 150°C)

PACKAGES

8-pin SOICN with exposed thermal pad (suffix LJ)

10-pin MSOP with exposed thermal pad (suffix LY)

16-pin TSSOP with exposed thermal pad (suffix LP)



Not to scale

DESCRIPTION

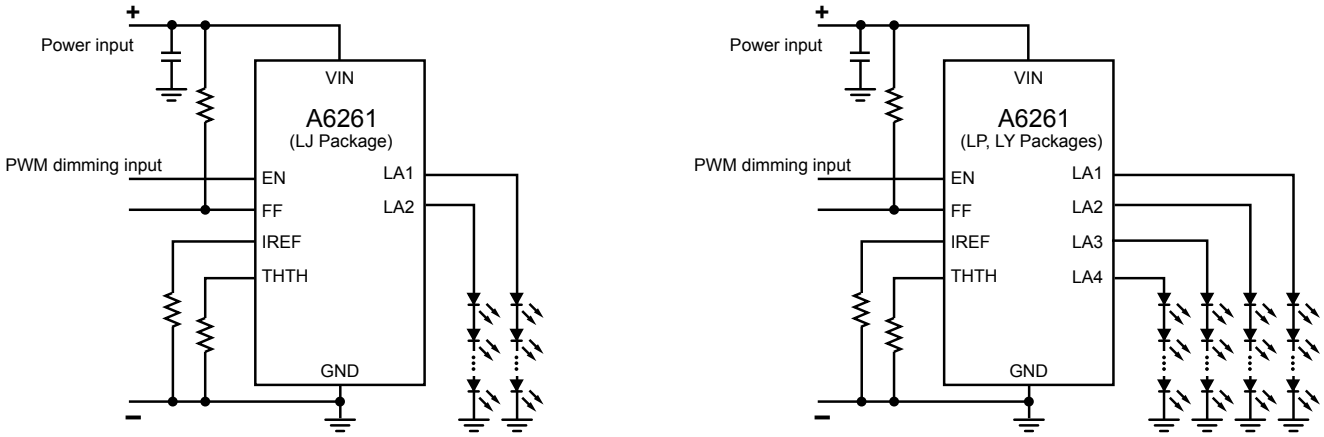
The A6261 is a linear, programmable current regulator providing up to 100 mA from each of four outputs (LP and LY) to drive arrays of high brightness LEDs. The regulated LED current from each output, accurate to 5%, is set by a single reference resistor. Current matching in each string is better than 10% without the use of ballast resistors. Driving LEDs with constant current ensures safe operation with maximum possible light output. The A6261 in the LJ package offers two pins with 200 mA each channel (A6261LJ-1) and with 100 mA and 200 mA maximum output current (A6261LJ).

Output control is provided by an enable input, giving direct control for PWM applications. Outputs can be connected in parallel or left unused as required.

Short detection is provided to protect the LEDs and the A6261 during a short-to-ground at any LED output pin. An open LED in any of the strings disables all outputs, but can be overridden. Shorted LED output pins or open LEDs are indicated by a fault flag.

A temperature monitor is included to reduce the LED drive current if the chip temperature exceeds a thermal threshold.

The device packages are an 8-pin SOICN (suffix LJ), a 10-pin MSOP (LY), and a 16-pin TSSOP (LP), all with exposed pad for enhanced thermal dissipation. They are lead (Pb) free, with 100% matte-tin leadframe plating.



Typical Application Diagrams

SELECTION GUIDE

Part Number	Ambient Operating Temperature, T_A (°C)	Packing	Current	Package
A6261KLJTR-T	–40 to 125	3000 pieces per 13-in. reel	LA1 = 200 mA LA2 = 100 mA	8-pin SOIC with exposed thermal pad
A6261KLJTR-T-1	–40 to 125	3000 pieces per 13-in. reel	LA1 = LA2 = 200 mA	8-pin SOIC with exposed thermal pad
A6261ELPTR-T	–40 to 85	4000 pieces per 13-in. reel	LA1-LA4 = 100 mA	16-pin TSSOP with exposed thermal pad
A6261KLPTR-T	–40 to 125	4000 pieces per 13-in. reel		
A6261KLYTR-T	–40 to 125	4000 pieces per 13-in. reel		10-pin MSOP with exposed thermal pad

ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Rating	Unit
Load Supply Voltage	V_{IN}		–0.3 to 50	V
Pin EN			–0.3 to 50	V
All LAx pins			–0.3 to 50	V
Pin FF			–0.3 to 50	V
Pins IREF, THTH			–0.3 to 6.5	V
Ambient Operating Temperature Range [2]	T_A	E temperature range	–40 to 85	°C
		K temperature range	–40 to 125	°C
Maximum Continuous Junction Temperature	T_J(max)		150	°C
Transient Junction Temperature	T_{tJ}	Overtemperature event not exceeding 10 seconds, lifetime duration not exceeding 10 hours, ensured by design characterization	175	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

[1] With respect to GND.
[2] Limited by power dissipation.

THERMAL CHARACTERISTICS [3]: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions*		Value	Unit
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	LJ package	On 4-layer PCB based on JEDEC standard	35	°C/W
			On 2-layer PCB with 0.8 in.^{2} of copper area each side	62	°C/W
		LP package	On 4-layer PCB based on JEDEC standard	34	°C/W
			On 2-layer PCB with 3.8 in.^{2} of copper area each side	43	°C/W
		LY package	On 4-layer PCB based on JEDEC standard	48	°C/W
			On 2-layer PCB with 2.5 in.^{2} of copper area each side	48	°C/W
Package Thermal Resistance (Junction to Pad)	$R_{\theta JP}$			2	°C/W

[3] To be verified by characterization for LP and LY. Additional thermal information available on the Allegro™ website.

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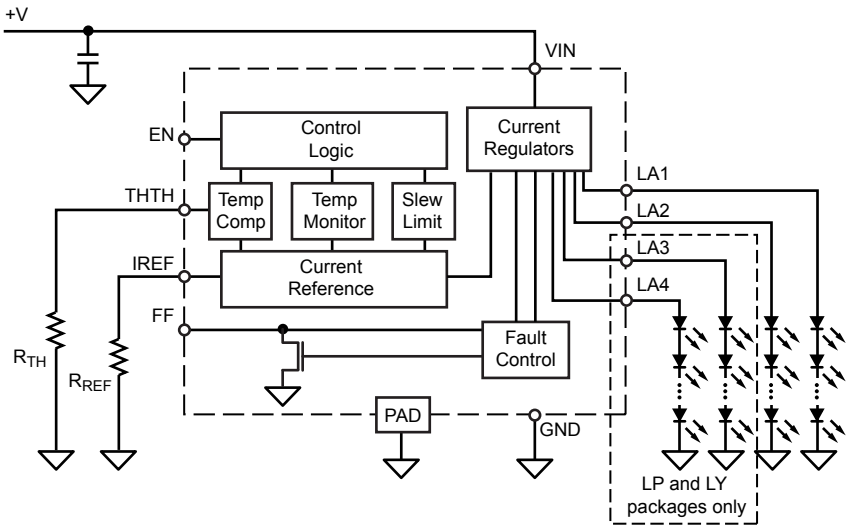
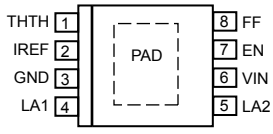
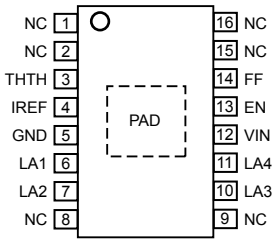


Functional Block Diagram

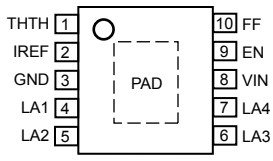
PINOUT DIAGRAMS AND TERMINAL LIST TABLE



LJ Package



LP Package



LY Package

Terminal List Table

Name	Number			Function
	LJ	LP	LY	
EN	7	13	9	Enable
FF	8	14	10	Fault output
GND	3	5	3	Ground reference
IREF	2	4	2	Current reference
LA1	4	6	4	LED anode (+) connection 1
LA2	5	7	5	LED anode (+) connection 2
LA3	–	10	6	LED anode (+) connection 3
LA4	–	11	7	LED anode (+) connection 4
NC	–	1,2,8, 9,15,16	–	No connection; connect to GND
PAD	–	–	–	Exposed thermal pad
THTH	1	3	1	Thermal threshold
VIN	6	12	8	Supply

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ELECTRICAL CHARACTERISTICS [1]: Valid at T_J = –40°C to 150°C, V_{IN} = 7 to 40 V, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY AND REFERENCE						
V_{IN} Functional Operating Range [2]	V_{IN}		6	–	50	V
V_{IN} Quiescent Current	I_{INQ}	All LAx pins connected to VIN	–	–	10	mA
V_{IN} Sleep Current	I_{INS}	EN = GND, V_{IN} = 16 V	–	–	10	µA
Startup Time	t_{ON}	V_{IN} > 7 V to I_{LA2} < –5 mA, R_{REF} = 125 Ω (except LJ-1 version); V_{IN} > 7 V to I_{LA2} < –10 mA, R_{REF} = 125 Ω (LJ-1 version)	5	20	30	µs
CURRENT REGULATION						
Reference Voltage	V_{IREF}	0.7 mA < I_{REF} < 8.8 mA	1.15	1.2	1.25	V
Reference Current Ratio	G_{H0}	LP and LY packages, I_{LAx} / I_{REF}	–	12.5	–	–
	G_{H1}	LJ package only I_{LA1} / $I_{REF,}$ LJ-1 package, I_{LAx}/I_{REF}	–	25	–	–
	G_{H2}	LJ package only I_{LA2} / I_{REF}	–	12.5	–	–
Current Accuracy [3]	E_{ILAx}	10% I_{LANx} > I_{LAx} > 100% I_{LANx}	–5	±4	5	%
		I_{LAx} = 10 mA, LJ-1 (200 mA × 2 channel) option [5]	–	10	–	%
Current Matching [4]	E_{IMLAx}	LP and LY packages only –20 mA > I_{LAx} > –100 mA, LJ-1 package only –40 mA > I_{LAx} > –200 mA, V_{LAx} match to within 1 V	–	5	10	%
Output Current	I_{LAx}	EN = high	–	G_{Hx} × I_{REF}	–	–
	I_{LAN0}	I_{REF} = 8 mA, EN = high, LP, LY and LA2 pin of LJ package	–105	–100	–95	mA
	I_{LAN1}	I_{REF} = 8 mA, EN = high, LJ-1 and LA1 pin of LJ package	–210	–200	–190	mA
Maximum Output Current	I_{LAxmax}	I_{REF} = 9.2 mA, EN = high, LP, LY and LA2 pin of LJ package	–	–	–110	mA
	I_{LA1max}	I_{REF} = 9.2 mA, EN = high, LJ-1 and LA1 pin of LJ package	–	–	–220	mA
Minimum Drop-Out Voltage	V_{DO}	V_{IN} – V_{LAx} , I_{LAx} = –100 mA, LP, LY and LA2 pin of LJ package	–	–	800	mV
		V_{IN} – V_{LAx} , I_{LAx} = –200 mA, LJ-1 and LA1 pin of LJ package	–	–	800	mV
		V_{IN} – V_{LAx} , I_{LAx} = –40 mA , LP, LY and LA2 pin of LJ package	–	–	660	mV
		V_{IN} – V_{LAx} , I_{LAx} = –80 mA, LJ-1 and LA1 pin of LJ package	–	–	660	mV
Output Disable Threshold	V_{ODIS}	V_{IN} – V_{LAx}	65	–	160	mV
Current Slew Time	t_{SL}	Current rising or falling between 10% and 90%	50	80	110	µs

Continued on the next page…

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ELECTRICAL CHARACTERISTICS [1] (continued): Valid at T_J = –40°C to 150°C, V_{IN} = 7 to 40 V, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
LOGIC INPUTS FF AND EN						
Input Low Voltage	V_{IL}		–	–	0.8	V
Input High Voltage	V_{IH}		2	–	–	V
Input Hysteresis (EN pin)	V_{Ihys}		150	350	–	mV
Pull-Down Resistor (EN pin)	R_{PD}		–	50	–	kΩ
Output Low Voltage (FF pin)	V_{OL}	I_{OL} = 1 mA	–	–	0.4	V
PROTECTION						
Short Detect Voltage	V_{SCD}	Measured at LAx	1.2	–	1.8	V
Short-Circuit Source Current	I_{SCS0}	Short present LAx to GND: LP, LY and LA2 pin of LJ package	–2	–0.8	–0.5	mA
	I_{SCS1}	Short present LAx to GND: LJ-1 and LA1 pin of LJ package	–4	–1.6	–1	mA
Short Release Voltage	V_{SCR}	Measured at LAx	–	–	1.9	V
Short Release Voltage Hysteresis	V_{SChys}	$V_{SCR} – V_{SCD}$	200	–	500	mV
Open-Load Detect Voltage	V_{OCD}	$V_{IN} – V_{LAx}$	170	–	450	mV
Open-Load Detect Delay	t_{OCD}		–	2	–	ms
Thermal Monitor Activation Temperature	T_{JM}	T_J with I_{SEN} = 90%, THTH pin is open	95	115	130	°C
Thermal Monitor Slope	dI_{SEN}/dT_J	I_{SEN} = 50%	–3.5	–2.5	–1.5	%/°C
Thermal Monitor Low Current Temperature	T_{JL}	T_J at I_{SEN} = 25%, THTH pin is open	120	135	150	°C
Overtemperature Shutdown	T_{JF}	Temperature increasing	–	170	–	°C
Overtemperature Hysteresis	T_{Jhys}	Recovery = $T_{JF} – T_{Jhys}$	–	15	–	°C

[1] For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.

[2] Function is correct but parameters are not guaranteed outside the general limits (7 to 40 V).

[3] When EN = high, $E_{ILAx} = 100 \times [(| I_{LAx} | \times R_{REF} / 15) – 1]$, with I_{LAx} in mA and R_{REF} in kΩ, for LP, LY and LA2 pin of LJ package.

[4] $E_{IMLA} = 100 \times \max (| I_{LAx} – I_{LA(AV)} |) / I_{LA(AV)}$, where $I_{LA(AV)}$ is the average current of all active outputs.

[5] Guaranteed by design and characterization, not production tested.

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FUNCTIONAL DESCRIPTION

The A6261 is a linear current regulator that is designed to provide drive current and protection for parallel strings of series-connected high brightness LEDs. The LP and LY options provide up to four matched programmable current outputs at up to 100 mA, and LJ-1 option provides two outputs with 200mA per channel, whereas the LJ option provides two outputs, LA1 = 200 mA and LA2 = 100 mA. All the outputs have low minimum dropout voltages below the main supply voltage. For 12 V power net applications, optimum performance is achieved when driving all strings of 1 to 3 series connected LEDs, at rated current per string.

The A6261 is specifically designed for use in applications where the LED current is controlled by a single logic input or a high-side switched supply. In addition, the A6261 disables all LEDs on detecting a single open LED.

Current regulation is maintained and the LEDs protected during a short-to-ground at any point in the LED string. A short-to-ground on any regulator output terminal will disable that output and set the fault flag. An open load on any output will set the fault flag and disable all outputs. Remaining outputs can be re-enabled by pulling the fault flag output low. Individual outputs can be disabled by connecting the output to VIN.

Integrated thermal management reduces the regulated current level at high internal junction temperatures to limit power dissipation.

Pin Functions

VIN Supply to the control circuit and current regulators. A small value ceramic bypass capacitor, typically 100 nF, should be connected from close to this pin to the GND pin.

GND. Ground reference connection. Should be connected directly to the negative supply.

EN. Logic input to enable LED current output. This provides a direct on/off action and can be used for direct PWM control.

IREF. 1.2 V reference to set current reference. Connect resistor, R_{REF}, to GND to set reference current.

THTH. Sets the thermal monitor threshold, T_{JM}, where the output current starts to reduce with increasing temperature. Connecting THTH directly to GND will disable the thermal monitor function.

LA[1:4]. Current source connected to the anode of the first LED in each string. Connect directly to VIN to disable the respective output. In this document, "LAx" indicates any one output of the ICs.

FF. Open drain fault flag, used with an external pull-up resistor, to indicate open, short, or overtemperature conditions. FF is inactive when a fault is present. During an open-load condition, FF can be pulled low to force the remaining outputs on.

LED Current Level

The LED current is controlled by four matching linear current regulators between the VIN pin and each of the LAx outputs. The basic equation that determines the nominal output current at each LAx pin is:

Given EN = high,

$$I_{REF} = \frac{1.2}{R_{REF}} \qquad (1)$$

and

$$I_{LAx} = G_{Hx} \times I_{REF} \qquad (2)$$

where I_{LAx} is in mA and R_{REF} is in kΩ.

The output current may be reduced from the set level by the thermal monitor circuit.

Conversely, the reference resistors may be calculated from:

$$R_{REF} = \frac{1.2 \times G_{Hx}}{I_{LAx}} \qquad (3)$$

where I_{LAx} is in mA and R_{REF} is in kΩ.

For example, where the required current is 90 mA per channel in LP or LY package the resistor value will be :

$$R_{REF} = \frac{15}{90} = 167\ \Omega$$

These equations completely define the output currents with respect to the setting resistors. However, for further reference, a more detailed description of the internal reference current calculations is included below.

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It is important to note that because the A6261 is a linear regulator, the maximum regulated current is limited by the power dissipation and the thermal management in the application. All current calculations assume adequate heatsinking for the dissipated power. Thermal management is at least as important as the electrical design in all applications. In high-current, high-ambient temperature applications, the thermal management is the most important aspect of the systems design. The application section below provides further detail on thermal management and the associated limitations.

Operation with Fewer LED Strings or Higher Currents

The A6261 may be configured to use fewer than four LED strings, either by connecting outputs together for higher currents, or by connecting the output directly to VIN to disable the regulator for that output. When a regulator is disabled, it will not indicate an open load and will not affect the fault flag or the operation of the remaining regulator outputs.

Sleep Mode

When EN is held low, the A6261 will be in shutdown mode and all sections will be in a low-power sleep mode. The input current will be typically less than 10 µA. This means that the complete circuit, including LEDs, may remain connected to the power supply under all conditions.

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Safety Features

The circuit includes several features to ensure safe operation and to protect the LEDs and the A6261:

- The current regulators between VIN and each LAx output provide a natural current limit due to the regulation.
- Each LAx output includes a short-to-ground detector that will disable the output to limit the dissipation.
- An open circuit on any output will disable all outputs.
- The thermal monitor reduces the regulated current as the temperature rises.
- Thermal shutdown completely disables the outputs under extreme overtemperature conditions.

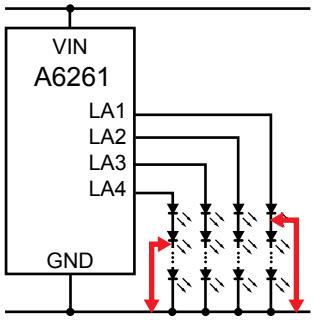
SHORT CIRCUIT DETECTION

A short-to-ground on any LED cathode (Figure 1A) will not result in a short fault condition. The current through the remaining LEDs will remain in regulation and the LEDs will be protected. Due to the difference in the voltage drop across the LEDs as a result of the short, the current matching in the A6261 may exceed the specified limits.

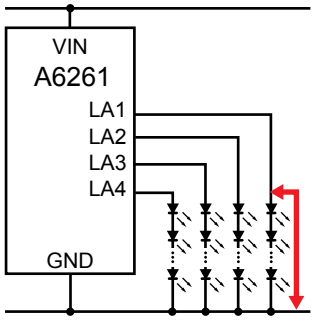
Any LAx output that is pulled below the short detect voltage (Figure 1B) will disable the regulator on that output and allow the fault flag, FF, to go high. A small current will be sourced from the disabled output to monitor the short and detect when it is removed. When the voltage at LAx rises above the short detect voltage, the fault flag will be removed and the regulator re-enabled.

A shorted LED (Figure 1C) will not result in a short fault condition. The current through the remaining LEDs will remain in regulation and the LEDs will be protected. Due to the difference in the voltage drop across the LEDs as a result of the short, the current matching in the A6261 may exceed the specified limits.

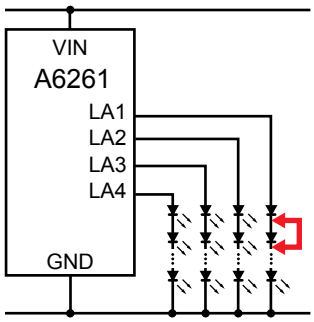
A short between LEDs in different strings (Figure 1D) will not result in a short fault condition. The current through the remaining LEDs will remain in regulation, and the LEDs will be protected. The current will be summed and shared by the affected strings. Current matching in the strings will then depend on the LED forward voltage differences.



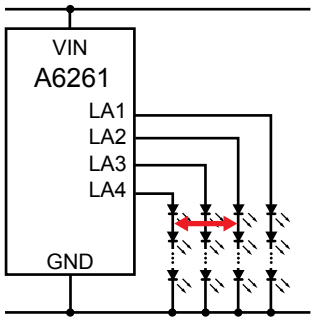
A. Any LED cathode short-to-ground. Current remains regulated in non-shorted LEDs. Matching may be affected. FF is low.



B. Any LAx output short-to-ground. Shorted output is disabled. Other outputs remain active. FF is high.



C. Shorted LEDs. Current remains regulated. Matching may be affected. Only the shorted LED is inactive. FF is low.



D. Short between LEDs in different strings. Current remains regulated. Current is summed and shared by affected strings. Intensity match dependent on voltage binning. FF is low.

Figure 1: Short-Circuit Conditions

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OPEN-LOAD DETECTION

An open-load condition is detected when the voltage across the regulator, $V_{IN} - V_{LAx}$, is less than the open-load detect voltage, V_{OCD}, but greater than the output disable threshold voltage, V_{ODIS}. When this condition is present for more than the open-load detect time, t_{OCD}, then all regulators will be disabled and the fault flag allowed to go high.

The regulators will remain disabled until either the power is cycled off and on, the EN input is taken low then high, or the fault flag, FF, is pulled low. If the power is cycled or EN is pulsed low, the regulators will start in the enabled state, unless disabled by tying the output to VIN, and the open-load detection timer will be reset. If the open load is still present the regulators will again be disabled after the open-load detect time.

Pulling the fault flag low will override the open-load fault action and all enabled regulators will be switched on. This state will be maintained while the fault flag is held low. If the fault flag is allowed to go high the A6261 will return to the open-load fault condition and will disable all regulators.

Each of the four regulators includes a limiter to ensure that the output voltage will not rise higher than the output disable threshold voltage below V_{IN} when driven by the regulator. This means that the voltage across the regulator will not be less than the output disable voltage, unless it is forced by connecting the LAx pin to VIN. However if a load becomes disconnected, the regulator will pull the LAx pin up to the limit, which will ensure that the voltage across the regulator, $V_{IN} - V_{LAx}$, is less than the open-load detect voltage, V_{OCD}.

Note that an open load may also be detected if the sum of the forward voltages of the LEDs in a string is close to or greater than the supply voltage on VIN.

TEMPERATURE MONITOR

A temperature monitor function, included in the A6261, reduces the LED current as the silicon junction temperature of the A6261 increases (see Figure 2). By mounting the A6261 on the same thermal substrate as the LEDs, this feature can also be used to limit the dissipation of the LEDs. As the junction temperature of the A6261 increases, the regulated current level is reduced, reducing the dissipated power in the A6261 and in the LEDs. The current is reduced from the 100% level at typically 2.5% per degree Celsius until the point at which the current drops to 25% of the full value, defined at T_{JL}. Above this temperature, the current will continue to reduce at a lower rate until the temperature reaches the overtemperature shutdown threshold temperature, T_{JF}.

The temperature at which the current reduction begins can be adjusted by changing the voltage on the THTH pin. When THTH is left open, the temperature at which the current reduction begins is defined as the thermal monitor activation temperature, T_{JM}, and is specified in the characteristics table at the 90% current level.

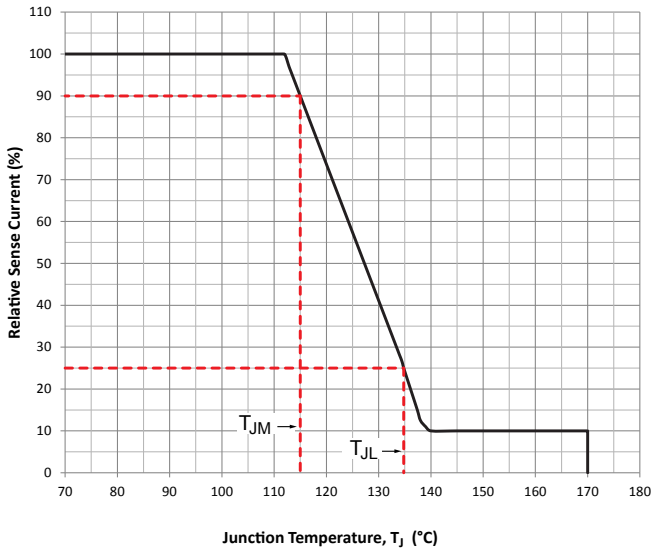

Figure 2: Temperature Monitor Current Reduction

Thermal monitor activation temperature can be set to a desired level by setting the voltage on the THTH pin (V_{THTH}). There is an internal 1 V source connected with a series resistor to the THTH pin inside the IC. A resistor connected between THTH and GND will reduce V_{THTH} and increase T_{JM}. A resistor connected between THTH and a reference supply greater than 1 V will increase V_{THTH} and reduce T_{JM}.

Figure 3a shows the relationship between T_{JM} and V_{THTH} while Figure 3b shows typical resistor values, either pull up or pull down, to set the voltage on THTH pin.

Now, based on the T_{JM} requirement, estimate the required V_{THTH} voltage from Figure 3a, and then, depending on the V_{THTH} value, decide the THTH pin resistor from Figure 3b. THTH pin resistor may either pull up or pull down depending on V_{THTH}.

As an example, if T_{JM} of 90°C is required, then from Figure 3a, V_{THTH} should be 1.115 V. To achieve this voltage, use Figure 3b to estimate THTH pin resistor (R_{TH}). If the pull-up voltage is 5 V, then a 211 kΩ resistor should be used. If the pull-up voltage is 3 V, use a 100 kΩ resistor.

In extreme cases, if the chip temperature exceeds the overtemperature limit, T_{JF} , all regulators will be disabled. The temperature will continue to be monitored and the regulators re-activated when the temperature drops below the threshold provided by the specified hysteresis.

Note that it is possible for the A6261 to transition rapidly between thermal shutdown and normal operation. This can happen if the thermal mass attached to the exposed thermal pad is small and T_{JM} is increased to close to the shutdown temperature.

The period of oscillation will depend on T_{JM}, the dissipated power, the thermal mass of any heatsink present, and the ambient temperature.

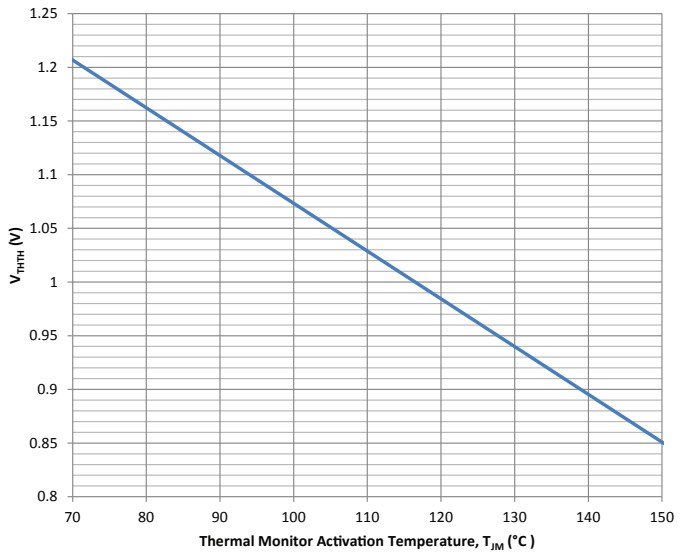

Figure 3a: Relationship Between T_{JM} and V_{THTH}

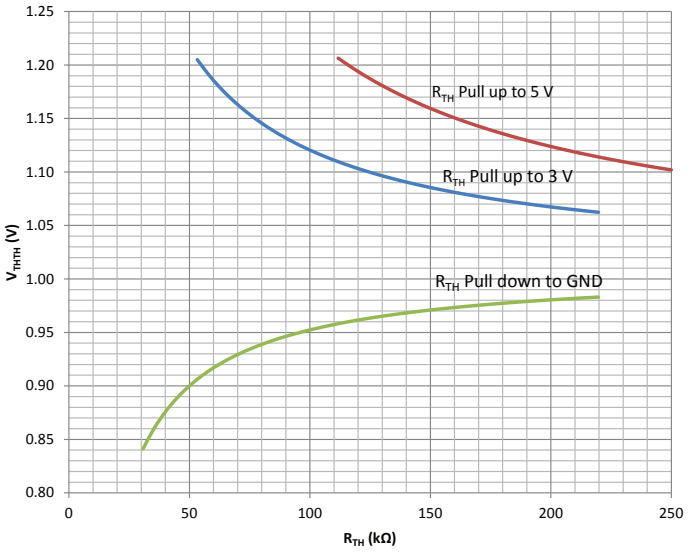

Figure 3b: Typical Resistor Values to Set Voltage on THTH Pin

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APPLICATION INFORMATION

Power Dissipation

The most critical design considerations when using a linear regulator such as the A6261 are the power produced internally as heat and the rate at which that heat can be dissipated.

There are three sources of power dissipation in the A6261:

- The quiescent power to run the control circuits
- The power in the reference circuit
- The power due to the regulator voltage drop

The elements relating to these dissipation sources are illustrated in Figure 4.

QUIESCENT POWER

The quiescent power is the product of the quiescent current, I_{INQ}, and the supply voltage, V_{IN}, and is not related to the regulated current. The quiescent power, P_Q, is therefore defined as:

$$P_Q = V_{IN} \times I_{INQ} \quad (4)$$

REFERENCE POWER

The reference circuit draws the reference current from the supply and passes it through the reference resistor to ground. The reference current is 8% of the output current on any one active output. The reference circuit power is the product of the reference current and the difference between the supply voltage and the reference voltage, typically 1.2 V. The reference power, P_{REF}, is therefore defined as:

$$P_{REF} = \frac{(V_{IN} - V_{REF}) \times V_{REF}}{R_{REF}} \quad (5)$$

REGULATOR POWER

In most application circuits, the largest dissipation will be produced by the output current regulators. The power dissipated in each current regulator is simply the product of the output current and the voltage drop across the regulator.

The total current regulator dissipation is the sum of the dissipation in each output regulator. The regulator power for each output is defined as:

$$P_{REGx} = (V_{IN} - V_{LEDx}) \times I_{LEDx} \quad (6)$$

where x is 1, 2, 3, or 4.

Note that the voltage drop across the regulator, V_{REG}, is always greater than the specified minimum dropout voltage, V_{DO}. The output current is regulated by making this voltage large enough to provide the voltage drop from the supply voltage to the total forward voltage of all LEDs in series, V_{LED}.

The total power dissipated in the A6261 is the sum of the quiescent power, the reference power, and the power in each of the four regulators:

$$P_{DIS} = P_Q + P_{REF} + P_{REGA} + P_{REGB} + P_{REGC} + P_{REGD} \quad (7)$$

The power that is dissipated in each string of LEDs is:

$$P_{LEDx} = V_{LEDx} \times I_{LEDx} \quad (8)$$

where x is A, B, C, or D, and V_{LEDx} is the voltage across all LEDs in the string.

From these equations (and as illustrated in Figure 5) it can be seen that, if the power in the A6261 is not limited, then it will increase as the supply voltage increases but the power in the LEDs will remain constant.

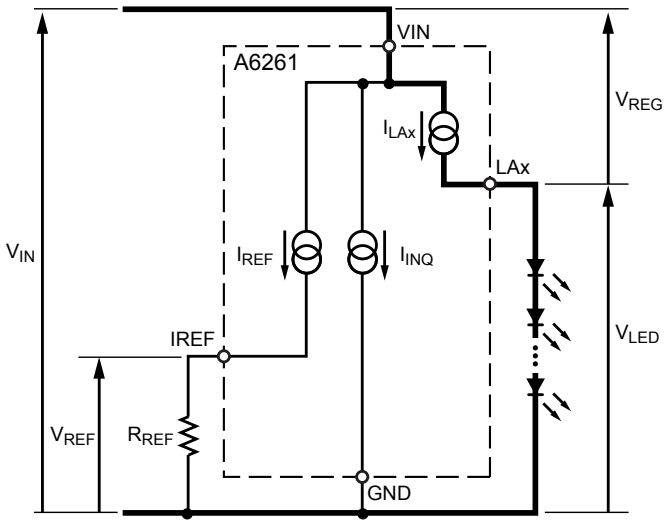

Figure 4: Internal Power Dissipation Sources

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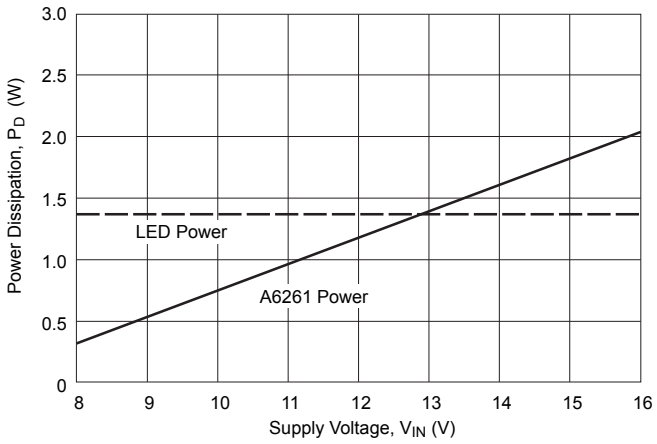

Figure 5: Power Dissipation versus Supply Voltage

Dissipation Limits

There are two features limiting the power that can be dissipated by the A6261: thermal shutdown and thermal foldback.

THERMAL SHUTDOWN

If the thermal foldback feature is disabled by connecting the THTH pin to GND, or if the thermal resistance from the A6261 to the ambient environment is high, then the silicon temperature will rise to the thermal shutdown threshold and the current will be disabled. After the current is disabled, the power dissipated will drop and the temperature will fall. When the temperature falls by the hysteresis of the thermal shutdown circuit, then the current will be re-enabled and the temperature will start to rise again. This cycle will repeat continuously until the ambient temperature drops or the A6261 is switched off. The period of this thermal shutdown cycle will depend on several electrical, mechanical, and thermal parameters and could be from a few milliseconds to a few seconds.

THERMAL FOLDBACK

If there is a good thermal connection to the A6261, then the thermal foldback feature will have time to act. This will limit the silicon temperature by reducing the regulated current and therefore the dissipation.

The thermal monitor will reduce the LED current as the temperature of the A6261 increases above the thermal monitor activation temperature, T_{JM}, as shown in Figure 6. The figure shows the operation of the A6261 with 4 strings of 3 red LEDs, each string running at 50 mA. The forward voltage of each LED is 2.3 V and the graph shows the current as the supply voltage increases from 14 to 17 V. As the supply voltage increases, without the thermal foldback feature, the current would remain at 50 mA, as shown by the dashed line. The solid line shows the resulting current decrease as the thermal foldback feature acts.

If the thermal foldback feature did not affect LED current, the current would increase the power dissipation and therefore the silicon temperature. The thermal foldback feature reduces power in the A6261 in order to limit the temperature increase, as shown in Figure 7. The figure shows the operation of the A6261 under the same conditions as Figure 6. That is, 4 strings of 3 red LEDs, each string running at 50 mA with each LED forward voltage at 2.3 V. The graph shows the temperature as the supply voltage

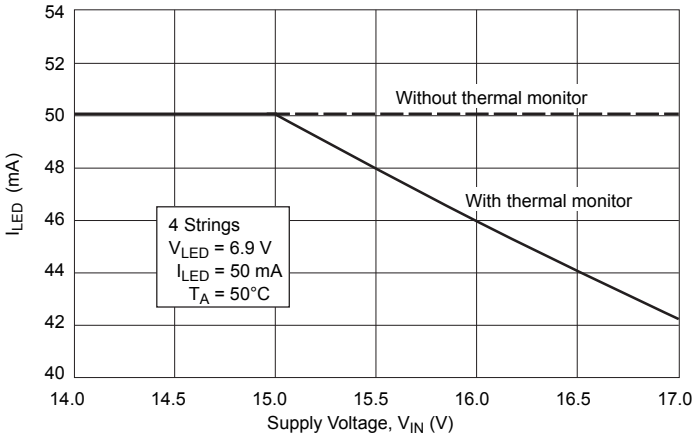

Figure 6: LED current versus Supply Voltage

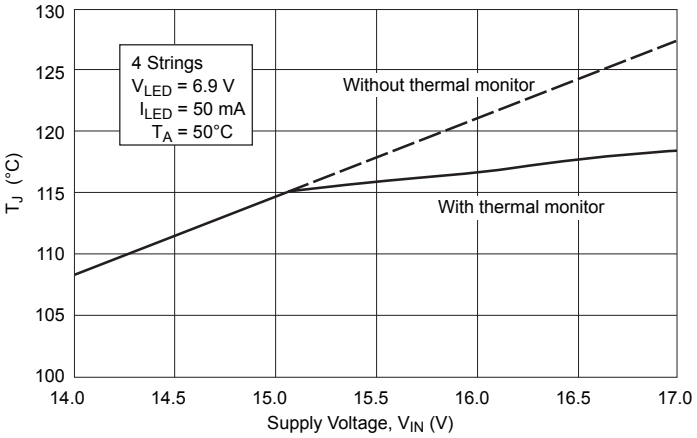

Figure 7: Junction Temperature versus Supply Voltage

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increases from 14 to 17 V. Without the thermal foldback feature, the temperature would continue to increase up to the thermal shutdown temperature as shown by the dashed line. The solid line shows the effect of the thermal foldback function in limiting the temperature rise.

Figures 6 and 7 show the thermal effects where the thermal resistance from the silicon to the ambient temperature is 40°C/W. Thermal performance can be enhanced further by using a significant amount of thermal vias as described below.

Thermal Dissipation

The amount of heat that can pass from the silicon of the A6261 to the ambient environment depends on the thermal resistance of the structures connected to the A6261. The thermal resistance, $R_{\theta JA}$, is a measure of the temperature rise created by the power dissipated and is usually measured in degrees Celsius per watt (°C/W).

The temperature rise, ΔT, is calculated from the power dissipated, P_D, and the thermal resistance, $R_{\theta JA}$, as:

$$\Delta T = P_D \times R_{\theta JA} \qquad (9)$$

A thermal resistance from silicon to ambient, $R_{\theta JA}$, of approximately 30°C/W (LP package) or 34°C/W (LY package), can be achieved by mounting the A6261 on a standard FR4 double-sided printed circuit board (PCB) with a copper area of a few square inches on each side of the board under the A6261. Multiple thermal vias, as shown in Figure 8, help to conduct the heat from the exposed pad of the A6261 to the copper on each side of the board. The thermal resistance can be reduced by using a metal substrate or by adding a heatsink.

Supply Voltage Limits

In some applications, the available supply voltage can vary over a two-to-one range— for example, emergency lighting systems using battery backup. In such systems is it necessary to design the application circuit such that the system meets the required performance targets over a specified voltage range.

To determine this range when using the A6261, there are two limiting conditions:

- For maximum supply voltage, the limiting factor is the power that can be dissipated from the regulator without exceeding the temperature at which the thermal foldback starts to reduce the output current below an acceptable level.

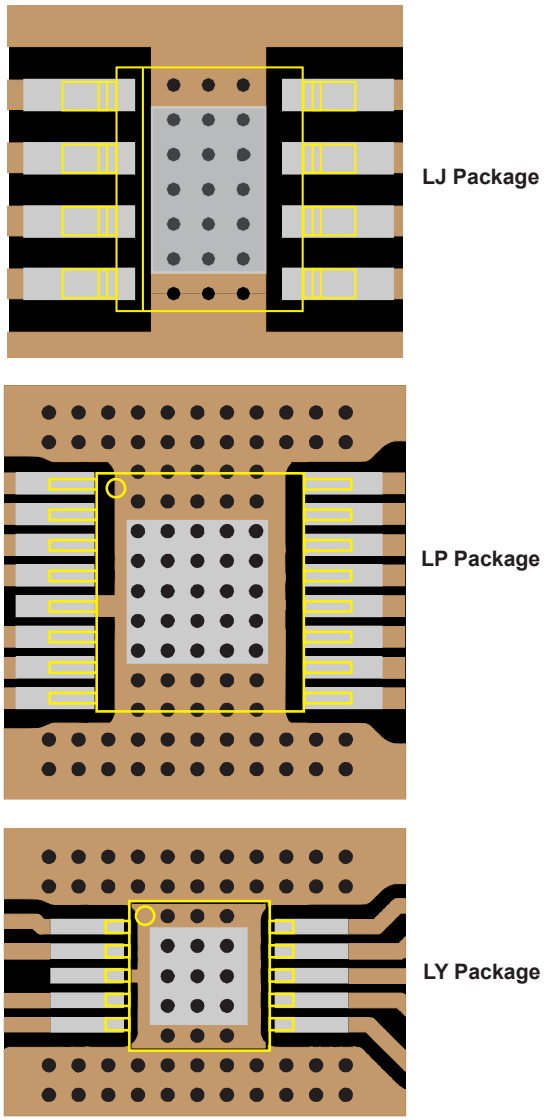


Figure 8: Board Via Layout for Thermal Dissipation

- For minimum supply voltage, the limiting factor is the maximum dropout voltage of the regulator, where the difference between the load voltage and the supply is insufficient for the regulator to maintain control over the output current.

MINIMUM SUPPLY LIMIT: REGULATOR SATURATION VOLTAGE

The supply voltage, V_{IN}, is always the sum of the voltage drop across the high-side regulator, V_{REG}, and the forward voltage of the LEDs in the string, V_{LED}, as shown in Figure 4.

V_{LED} is constant for a given current and does not vary with supply voltage. Therefore, V_{REG} provides the variable difference between V_{LED} and V_{IN}. V_{REG} has a minimum value below which the regulator can no longer be guaranteed to maintain the output current within the specified accuracy. This level is defined as the regulator dropout voltage, V_{DO}.

The minimum supply voltage, below which the LED current does not meet the specified accuracy, is therefore determined by the sum of the minimum dropout voltage, V_{DO}, and the forward voltage of the LEDs in the string, V_{LED}. The supply voltage must always be greater than this value and the minimum specified supply voltage, that is:

$$V_{IN} > V_{DO} + V_{LED},$$

and

$$V_{IN} > V_{IN}(min) \qquad (10)$$

As an example, consider the configuration used in Figures 6 and 7 above, namely 4 strings of 3 red LEDs, each string running at 50 mA, with each LED forward voltage at 2.3 V. The minimum supply voltage will be approximately:

$$V_{IN}(\text{min}) = 0.55 + (3 \times 2.3) = 7.45 \text{ V}$$

MAXIMUM SUPPLY LIMIT: THERMAL LIMITATION

As described above, when the thermal monitor reaches the activation temperature, T_{JM} (due to increased power dissipation as the supply voltage rises), the thermal foldback feature causes the output current to decrease. The maximum supply voltage is therefore defined as the voltage above which the LED current drops below the acceptable minimum.

This can be estimated by determining the maximum power that can be dissipated before the internal (junction) temperature of the A6261 reaches T_{JM}.

Note that, if the thermal monitor circuit is disabled (by connecting the THTH pin to GND), then the maximum supply limit will be determined by the specified maximum continuous operating temperature, 150°C.

The maximum power dissipation is therefore defined as:

$$P_D(\text{max}) = \frac{\Delta T}{R_{\theta JA}} \qquad (11)$$

where ΔT is difference between the thermal monitor activation temperature, T_{JM}, of the A6261 and the maximum ambient temperature, T_A(max), and $R_{\theta JA}$ is the thermal resistance from the internal junctions in the silicon to the ambient environment.

If minimum LED current is not a critical factor, then the maximum voltage is simply the absolute maximum specified in the parameter tables above.

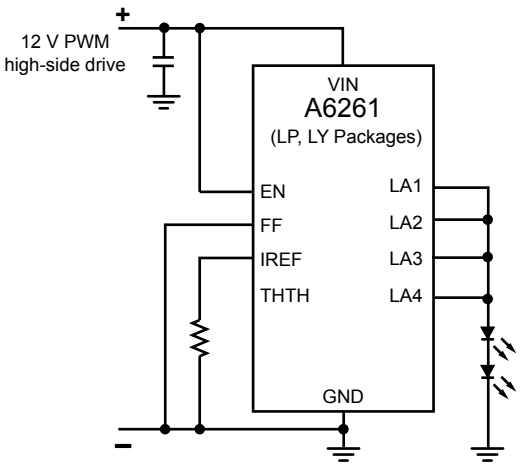
Application Examples

In some filament bulb replacement applications, the supply may be provided by a PWM-driven, high-side switch. The A6261 can be used in this application by simply connecting EN to VIN.

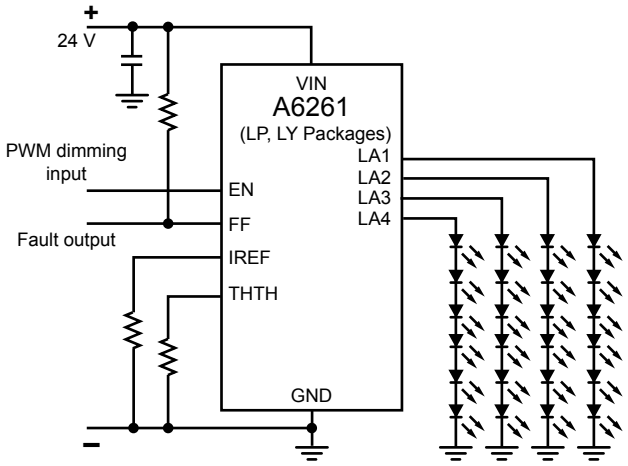
If neither fault action nor fault reporting is required, then FF should be tied to ground.

When power is applied, there will be a short startup delay, t_{ON}, before the current starts to rise. The current rise time will be limited by the internal current slew rate control.

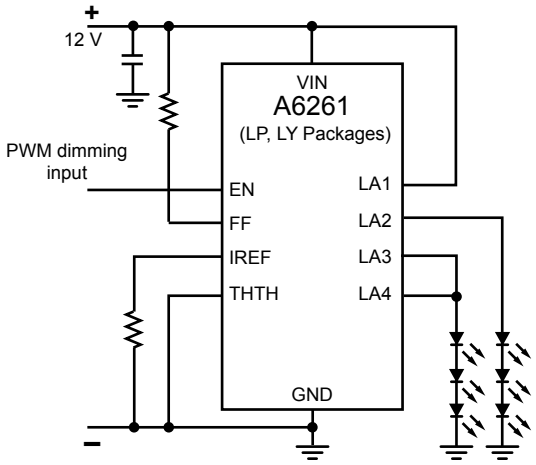
The application circuit options in Figure 9 show operation with a higher voltage supply and with combinations of outputs tied together and disabled.



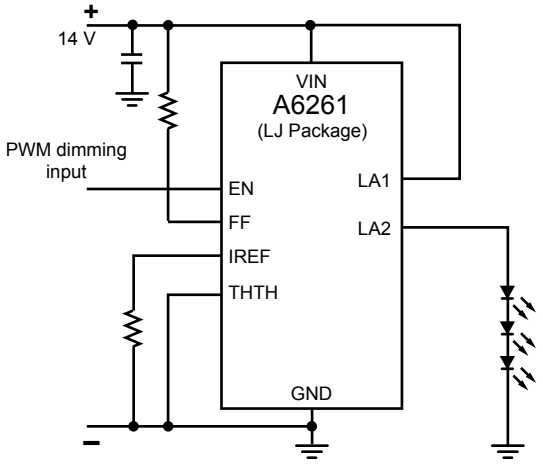
A. High brightness (HB) LED incandescent lamp replacement



B. Higher voltage operation



C. Mix of output combinations



D. A6261LJ: Single output with 100mA. For 200 mA single output, connect LA2 to VIN and LEDs to LA1.

Figure 9: Typical Applications with Various Supply and Output Options.

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Binning Resistor Arrangement

An external binning resistor can be connected in series with the IREF pin to set appropriate current through various LED batches. A filter capacitor of 100 nF should be placed after R_{REF1} as shown in Figure 10.

$$I_{LAx}(min) = (1.2 \times G_{HX}) \div (R_{REF1} + R_{REF2}) \quad (12)$$

$$I_{LAx}(max) = (1.2 \times G_{HX}) \div R_{REF1} \quad (13)$$

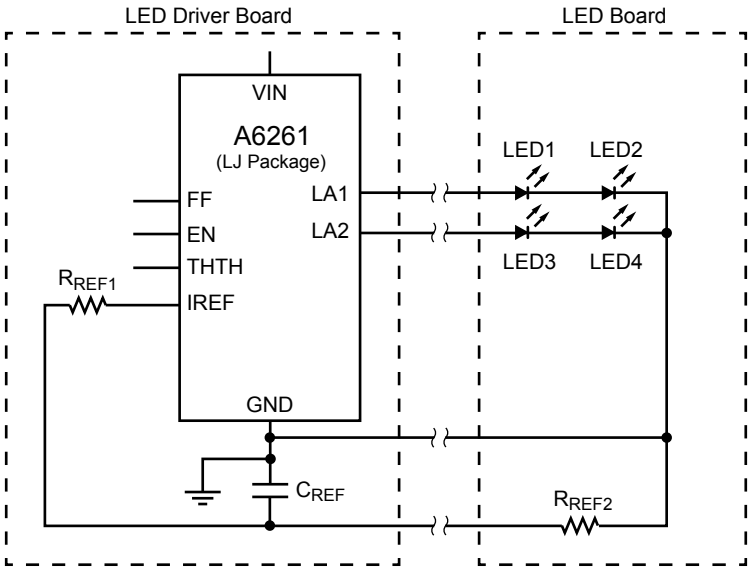

Figure 10: Application Circuit for Binning – Current-setting resistor (R_{REF2}) can be placed on LED board for different bins of LEDs.

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PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use

(Reference MS-012BA)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

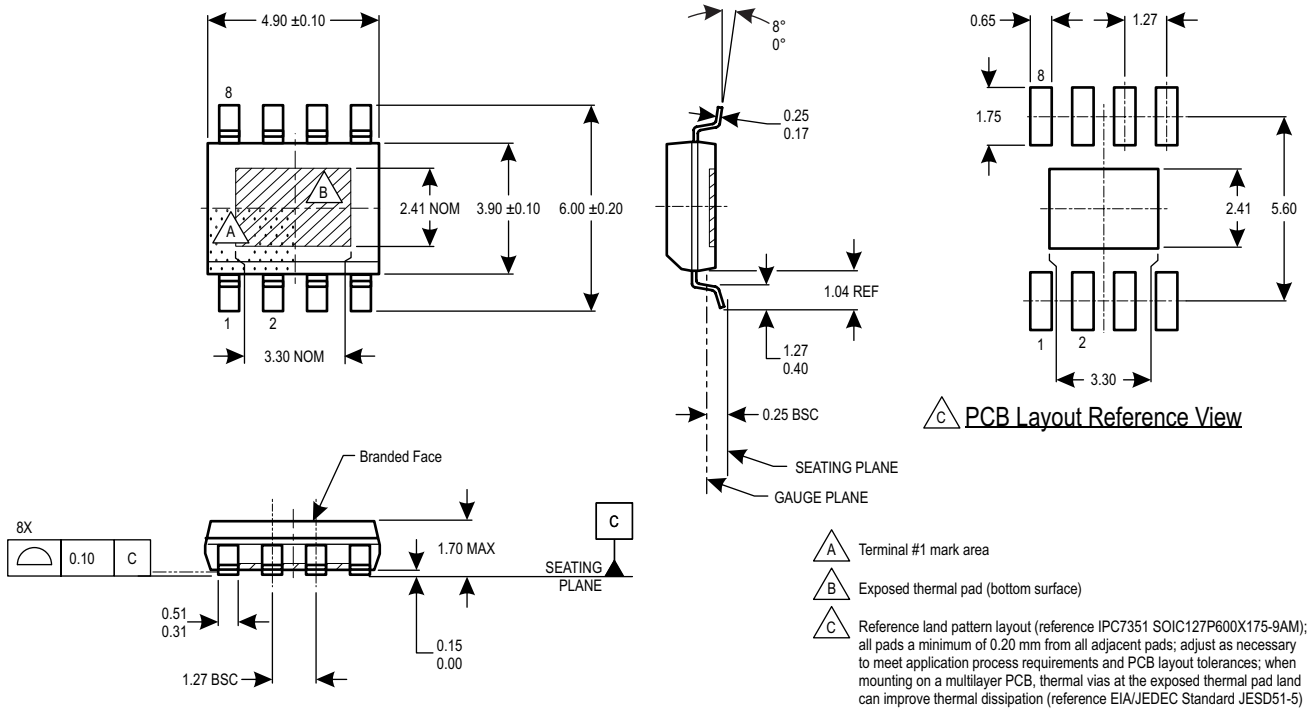

Figure 11: Package LJ, 8-Pin SOICN with Exposed Thermal Pad

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(Reference MO-153 ABT)
Dimensions in millimeters. NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

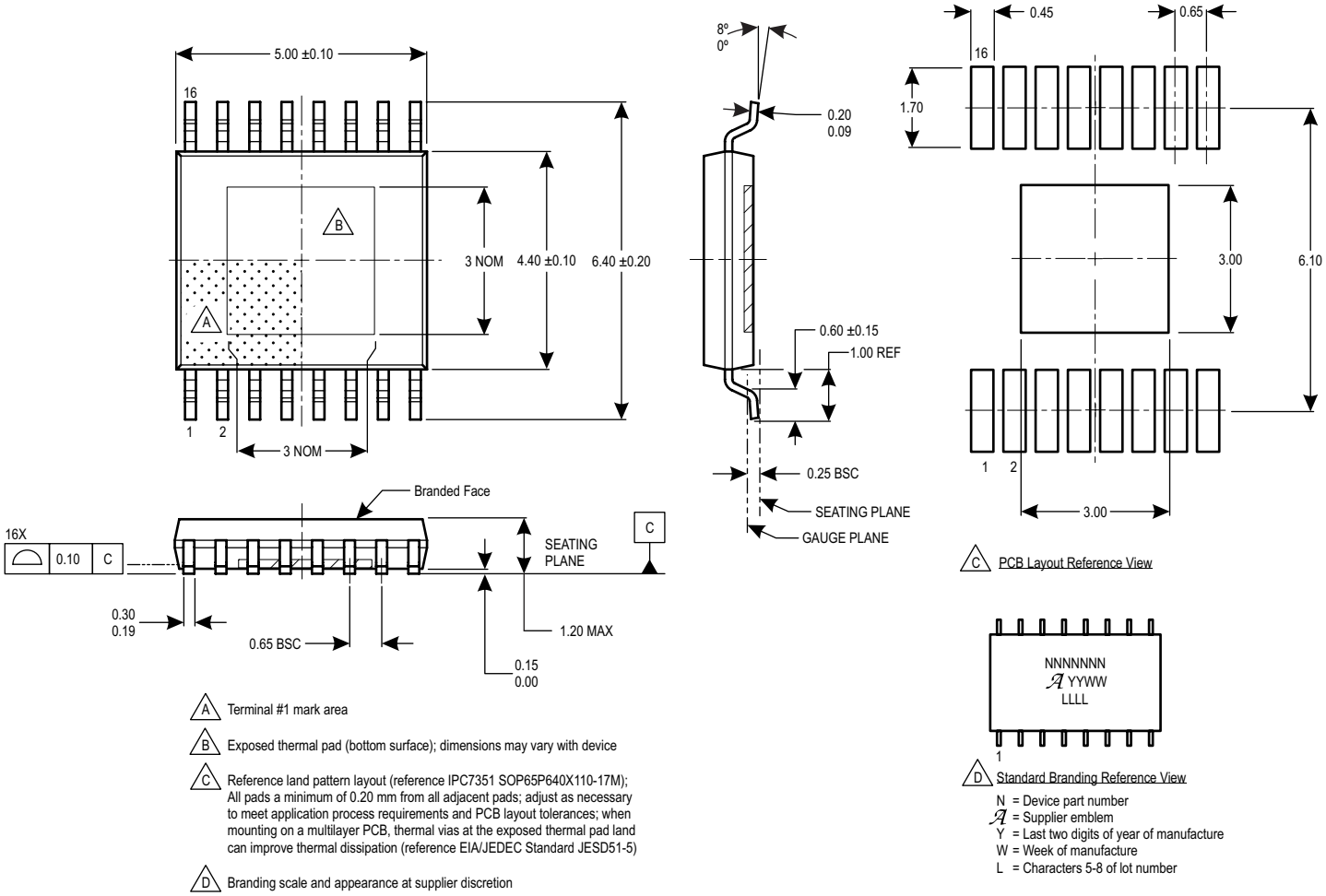

Figure 12: Package LP, 16-Pin TSSOP with Exposed Thermal Pad

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For Reference Only – Not for Tooling Use

(Reference JEDEC MO-187)
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Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

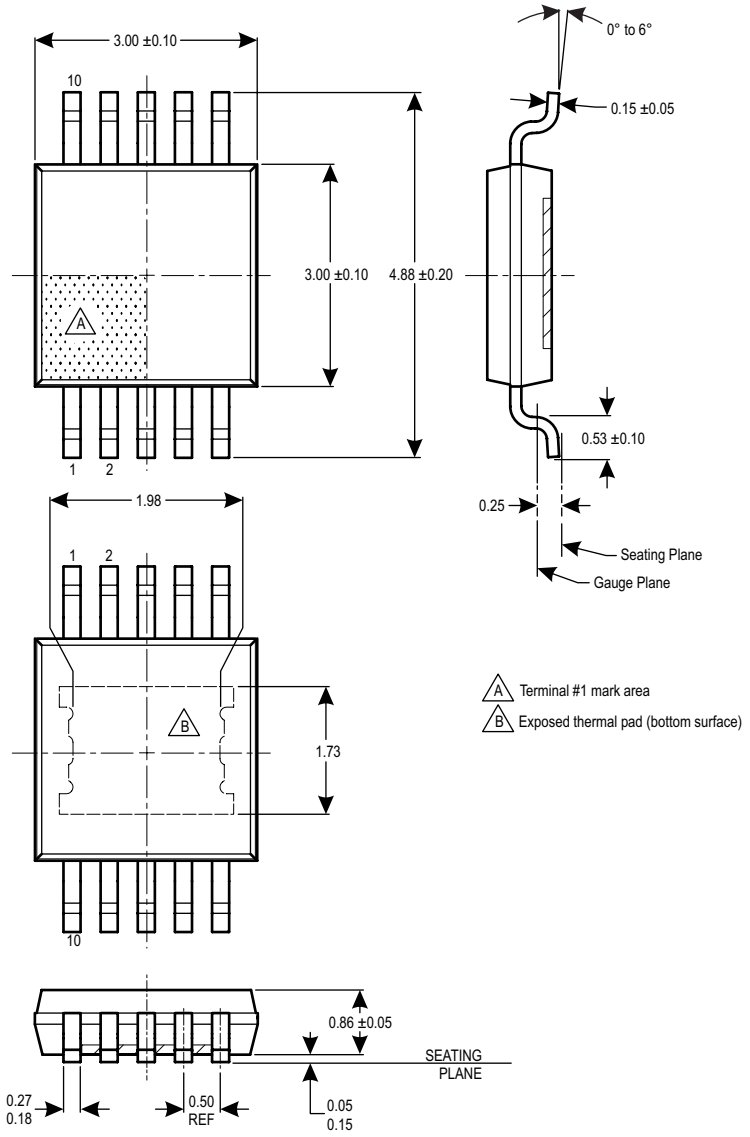

Figure 13: Package LY, 10-Pin MSOP with Exposed Thermal Pad

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Revision History

Number	Date	Description
8	September 10, 2013	Add LJ package
9	December 6, 2014	Add LJ-1 package; revised Selection Guide
10	June 25, 2015	Temperature Monitor text on page 9 updated to match EC table: derating slope is –2.5% per °C
11	September 30, 2015	Removed Contact Factory status from A6261KLJTR-T-1; THTH pin resistor (R_{THTH}) selection description modified; Binning resistor application note added; figure 2 updated.
12	July 28, 2016	Updated Figure 10
13	January 8, 2018	Updated Current Accuracy characteristic in EC table (page 4)
14	January 21, 2019	Minor editorial updates

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