PSMN1R4-40YLD

N-channel 40 V, 1.4 mΩ, 240 A logic level MOSFET in LFPAK56 using NextPower-S3 technology

14 March 2019 — Product data sheet

1. General description

240 Amp, logic level gate drive N-channel enhancement mode MOSFET in 175 °C LFPAK56 package using advanced TrenchMOS Superjunction technology. This product has been designed and qualified for high performance power switching applications.

2. Features and benefits

- 240 A capability
- Avalanche rated, 100% tested at I_{AS} = 190 A
- NextPower-S3 technology delivers 'superfast switching with soft recovery'
- Low Q_{RR}, Q_G and Q_{GD} for high system efficiency and low EMI designs
- Schottky-Plus body-diode, gives soft switching without the associated high I_{DSS} leakage
- Optimised for 4.5 V gate drive utilising NextPower-S3 Superjunction technology
- High reliability LFPAK (Power SO8) package, copper-clip, solder die attach and qualified to 175 °C
- Exposed leads can be wave soldered, visual solder joint inspection and high quality solder joints
- Low parasitic inductance and resistance

3. Applications

- Synchronous rectification
- DC-to-DC converters
- High performance & high efficiency server power supply
- Motor control
- Power OR-ing

4. Quick reference data

Table 1. Quick reference data

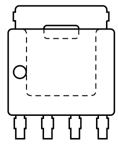
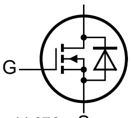
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	40	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	-	240	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	238	W
T_j	junction temperature			-55	-	175	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C; Fig. 10		-	1.38	1.85	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 10		-	1.12	1.4	mΩ
Dynamic characteristics							

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 20 V; V_{GS} = 4.5 V; Fig. 12; Fig. 13		-	13	26	nC
$Q_{G(tot)}$	total gate charge			-	45	65	nC

[1] 240A continuous current has been successfully demonstrated during application test. Practically, the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	mb  1 2 3 4 **LFPAK56; Power-SO8 (SOT669)**	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R4-40YLD	LFPAK56; Power-SO8	Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN1R4-40YLD	1D440L

8. Limiting values

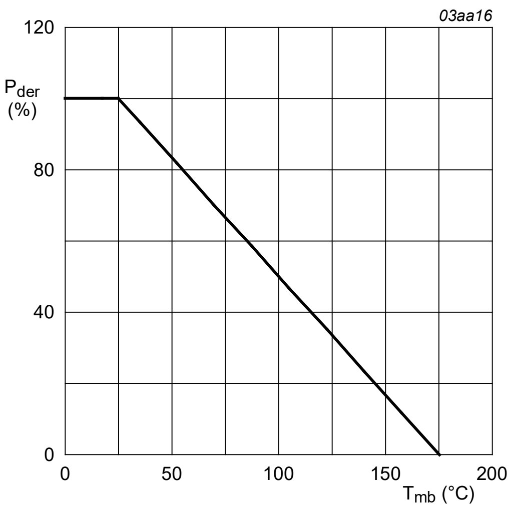
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	40	V
V_{DSM}	peak drain-source voltage	t_p ≤ 20 ns; f ≤ 500 kHz; $E_{DS(AL)}$ ≤ 200 nJ; pulsed		-	45	V
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ		-	40	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	238	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	240	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 2		-	214	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 3		-	1201	A
T_{stg}	storage temperature			-55	175	°C

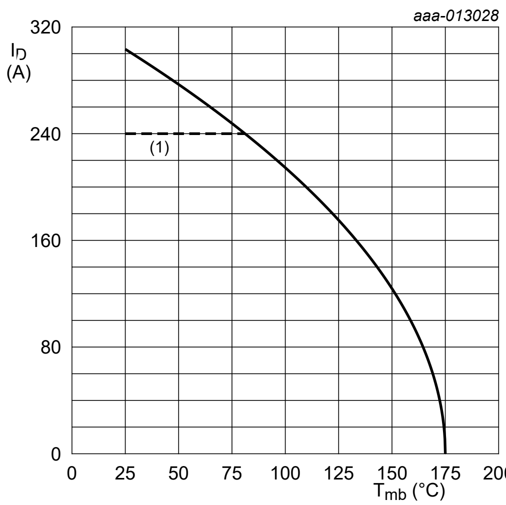
Symbol	Parameter	Conditions		Min	Max	Unit
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
V_{ESD}	electrostatic discharge voltage	HBM		2	-	kV
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	198.6	A
I_{SM}	peak source current	pulsed; $t_p \leq$ 10 µs; T_{mb} = 25 °C		-	1201	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 74 A; $V_{sup} \leq$ 40 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; t_p = 0.23 ms	[2]	-	446	mJ
		I_D = 25 A; $V_{sup} \leq$ 40 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; t_p = 2.52 ms	[2]	-	1641	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} \leq$ 40 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; R_{GS} = 50 Ω	[2]	-	190	A

[1] 240A continuous current has been successfully demonstrated during application test. Practically, the current will be limited by PCB, thermal design and operating temperature.
[2] Protected by 100% test



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



(1) 240A Continuous current has been successfully demonstrate during application tests. Practically the current will be limited by PCB, thermal design and operation temperature.
$V_{GS} \geq 10$ V

Fig. 2. Continuous drain current as a function of mounting base temperature

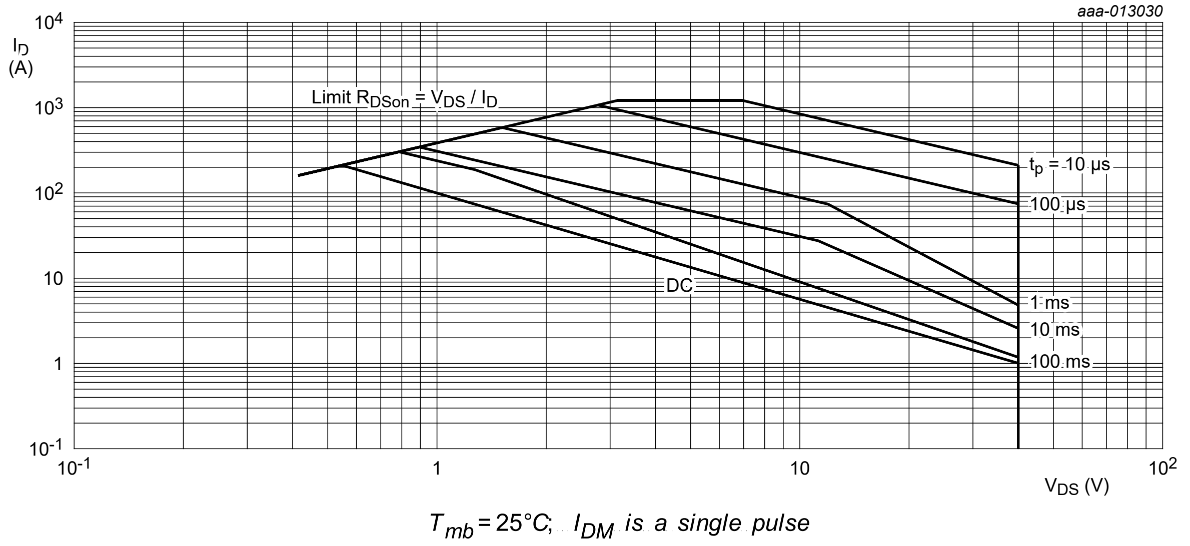


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4		-	0.56	0.63	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 5		-	50	-	K/W
		Fig. 6		-	125	-	K/W

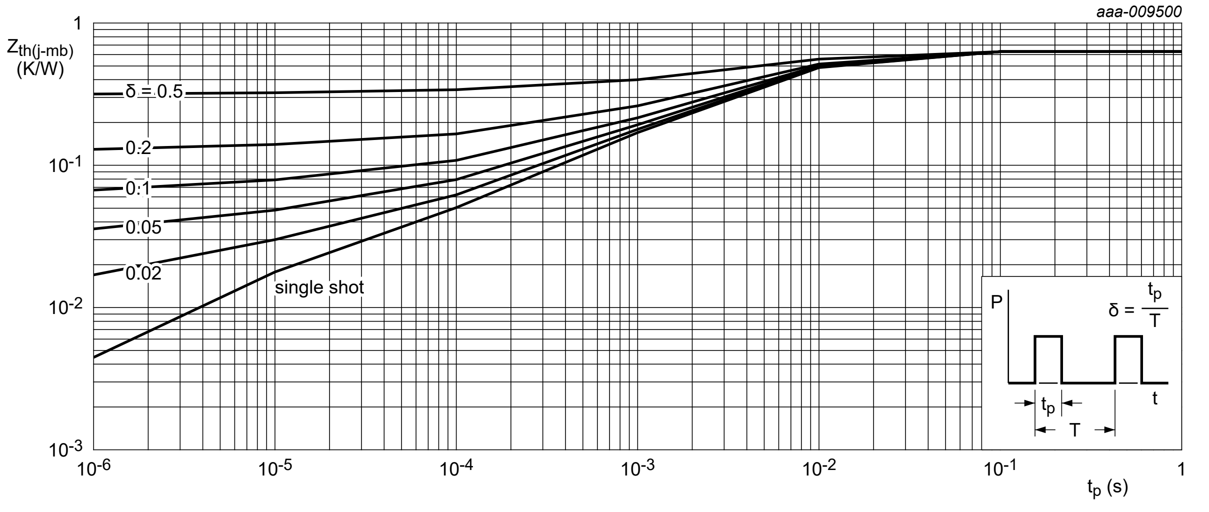


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

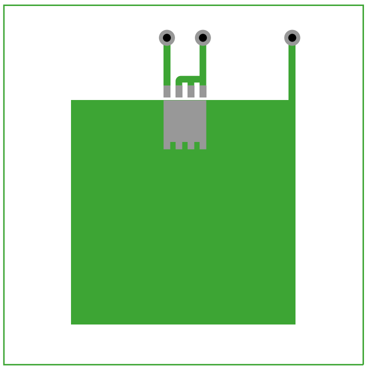


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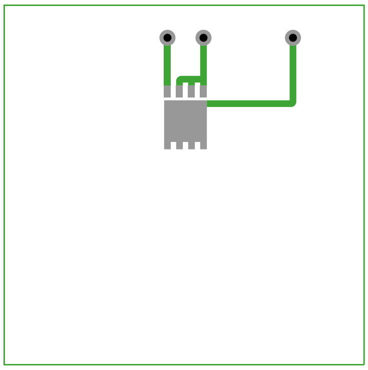
Fig. 5. PCB layout for thermal resistance junction to ambient 1” square pad; FR4 Board; 2oz copper



aaa-005751

Fig. 6. PCB layout for thermal resistance junction to ambient minimum footprint;FR4 board; 2oz copper

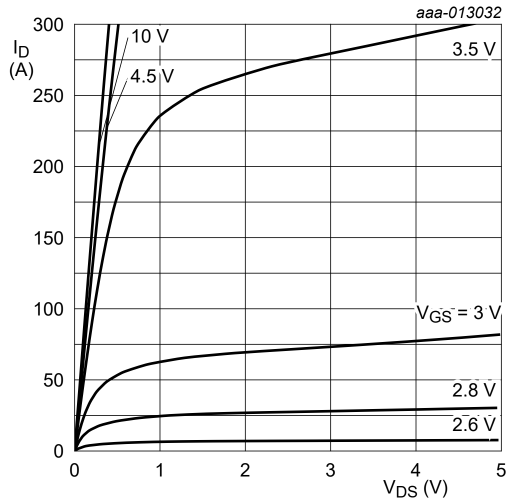
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		40	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C		1.05	1.7	2.2	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	25 °C ≤ T_j ≤ 150 °C		-	-4.8	-	mV/K
I_{DSS}	drain leakage current	V_{DS} = 32 V; V_{GS} = 0 V; T_j = 25 °C		-	-	1	µA
		V_{DS} = 32 V; V_{GS} = 0 V; T_j = 125 °C		-	12	-	µA
I_{GSS}	gate leakage current	V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
		V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 10		-	1.12	1.4	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; Fig. 10; Fig. 11		-	-	2.65	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C; Fig. 10		-	1.38	1.85	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; T_j = 175 °C; Fig. 10; Fig. 11		-	-	3.4	mΩ
R_G	gate resistance	f = 1 MHz		-	1.1	3.43	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 20 V; V_{GS} = 10 V; Fig. 12; Fig. 13		-	96	143	nC
		I_D = 25 A; V_{DS} = 20 V; V_{GS} = 4.5 V; Fig. 12; Fig. 13		-	45	65	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V		-	85	-	nC
Q_{GS}	gate-source charge	I_D = 25 A; V_{DS} = 20 V; V_{GS} = 4.5 V; Fig. 12; Fig. 13		-	15	25	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	9	-	nC

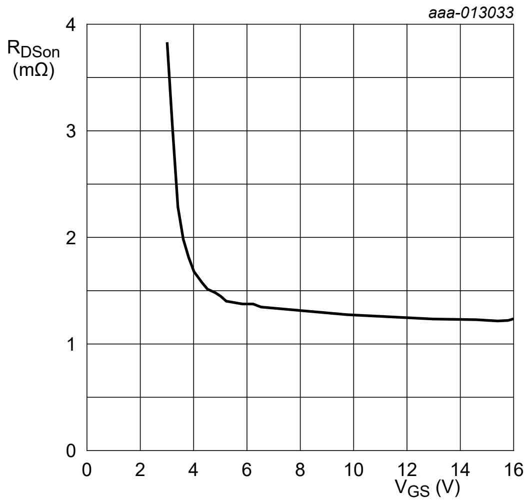
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	6	-	nC
Q_{GD}	gate-drain charge			-	13	26	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 25 A; V_{DS} = 20 V; Fig. 12; Fig. 13		-	2.7	-	V
C_{iss}	input capacitance	V_{DS} = 20 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 14		-	6661	10413	pF
C_{oss}	output capacitance			-	1543	2309	pF
C_{rss}	reverse transfer capacitance			-	299	658	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 20 V; R_L = 0.8 Ω; V_{GS} = 4.5 V; $R_{G(ext)}$ = 5 Ω		-	39	-	ns
t_r	rise time			-	49	-	ns
$t_{d(off)}$	turn-off delay time			-	47	-	ns
t_f	fall time			-	30	-	ns
Q_{oss}	output charge	V_{GS} = 0 V; V_{DS} = 20 V; f = 1 MHz; T_j = 25 °C		-	50	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 15		-	0.78	1.2	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; Fig. 16		-	47	-	ns
Q_r	recovered charge		[1]	-	61	-	nC
t_a	reverse recovery rise time			-	25.4	-	ns
t_b	reverse recovery fall time			-	21.7	-	ns

[1] includes capacitive recovery



T_j = 25 °C

Fig. 7. Output characteristics; drain current as a function of drain-source voltage; typical values



T_j = 25°C; I_D = 25A

Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

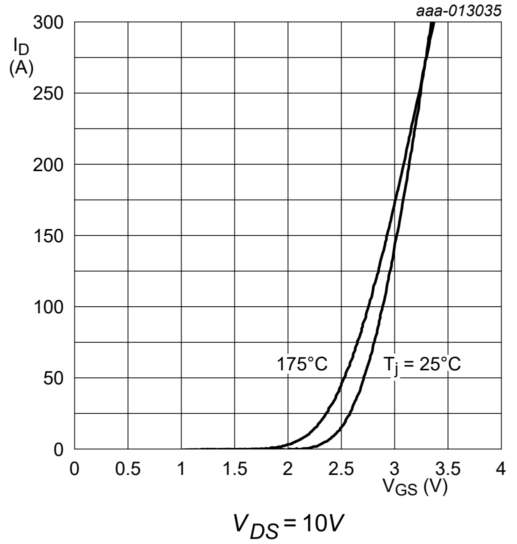


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

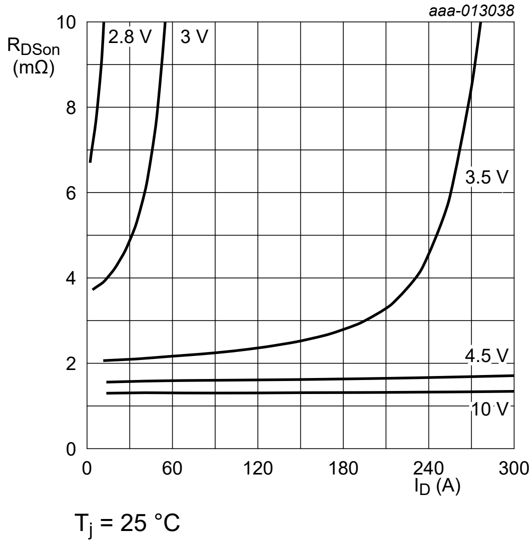
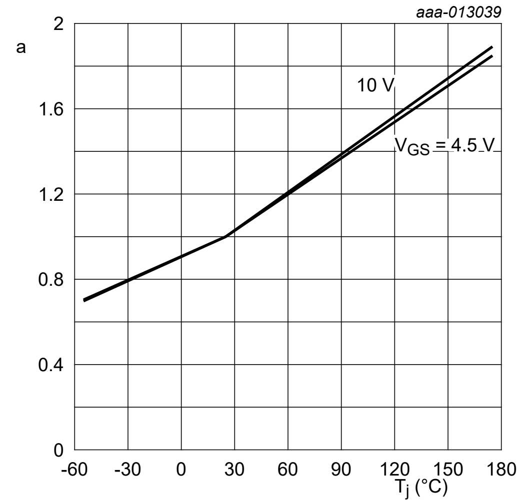


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon\ (25°C)}}$$

Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

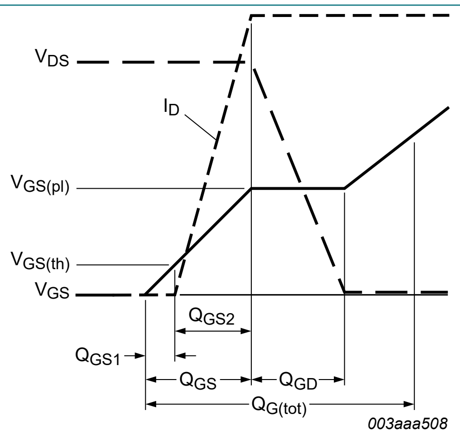
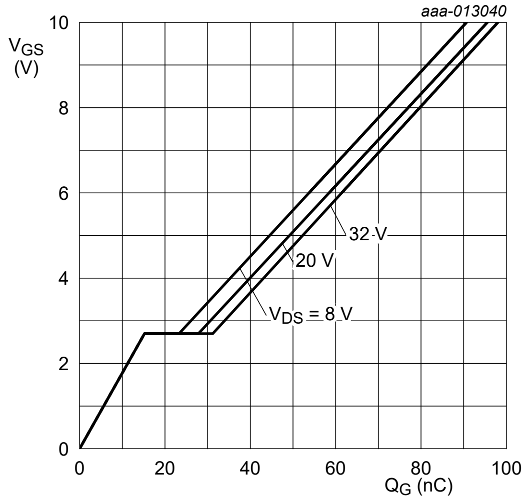
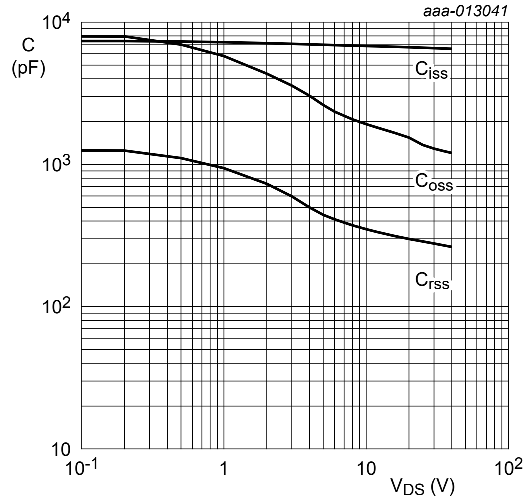


Fig. 12. Gate charge waveform definitions



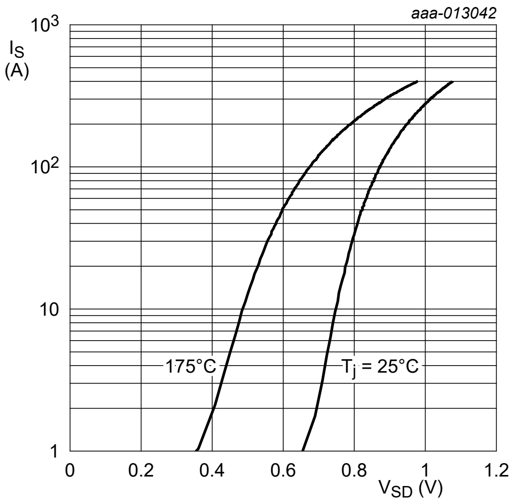
$T_j = 25°C$; $I_D = 25A$

Fig. 13. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0V$; $f = 1MHz$

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0V$

Fig. 15. Source current as a function of source-drain voltage; typical values

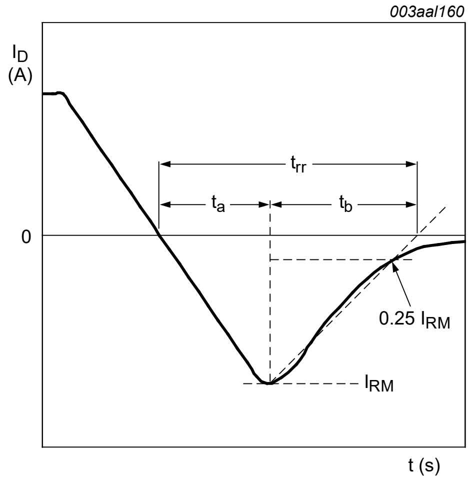
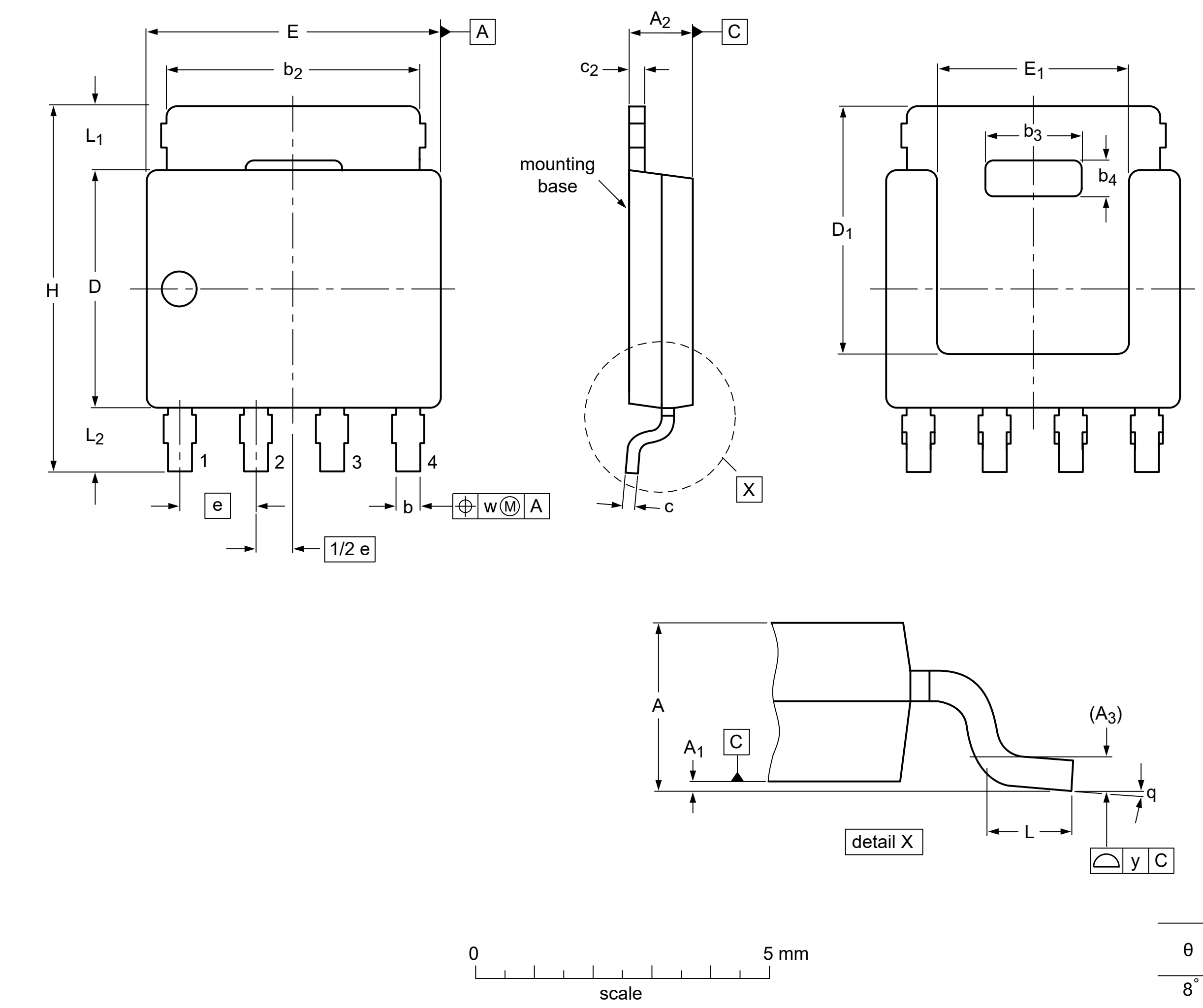


Fig. 16. Reverse recovery timing definition

11. Package outline

Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads **SOT669**



Dimensions (mm are the original dimensions)

Unit(1)		A	A_1	A_2	A_3	b	b_2	b_3	b_4	c	c_2	D(1)	D_1(1)	E(1)	E_1(1)	e	H	L	L_1	L_2	w	y	θ
mm	max	1.20	0.15	1.10		0.50	4.41	2.2	0.9	0.25	0.30	4.10	4.20	5.0	3.3		6.2	0.85	1.3	1.3			8°
	nom				0.25											1.27					0.25	0.1	
	min	1.01	0.00	0.95		0.35	3.62	2.0	0.7	0.19	0.24	3.80		4.8	3.1		5.8	0.40	0.8	0.8			0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

sot669_po

Outline version	References IEC	JEDEC	JEITA		European projection	Issue date
SOT669		MO-235				~~11-03-25~~ 13-02-27

Fig. 17. Package outline LFPAK56; Power-SO8 (SOT669)

12. Soldering

Footprint information for reflow soldering **SOT669**

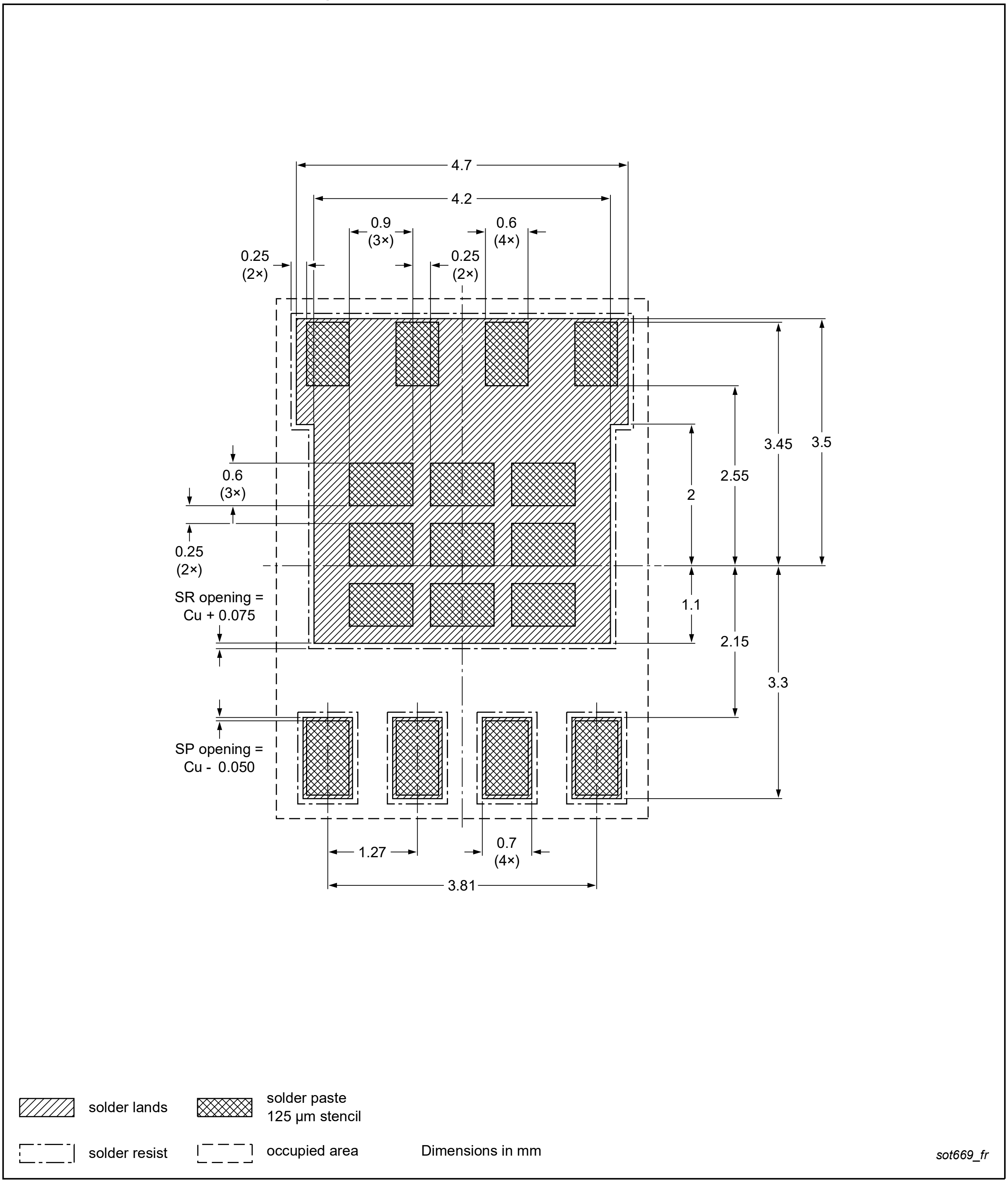


Fig. 18. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT669)

Wave soldering footprint information for LFPAK56 package **SOT669**

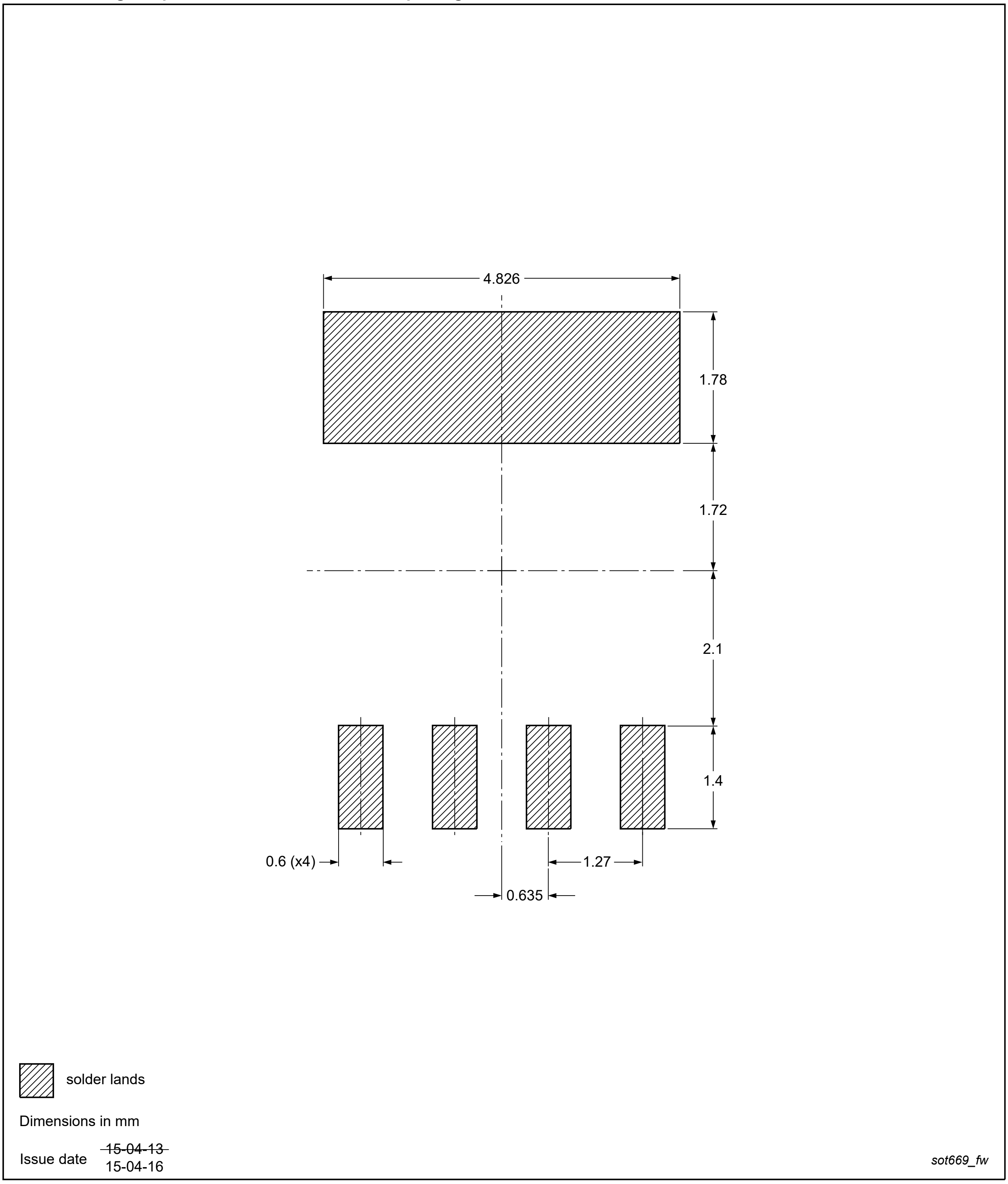


Fig. 19. Wave soldering footprint for LFPAK56; Power-SO8 (SOT669)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
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