Keywords: PRM, HDLC

APPLICATION NOTE 6505

HANDLING PERFORMANCE REPORT MESSAGES IN THE DS2155

By: Aparna K P

Abstract: This application note discusses transmitting/receiving a PRM as an HDLC message over T1 FDL and time slots. It also gives a detailed explanation on the configuration of HDLC engines in the DS2155.

Introduction

This application note gives a detailed explanation on handling a Performance Report Message (PRM) in the DS2155 and how to transmit or receive a PRM as an HDLC message over a T1 Facilities Data Link (FDL).

The FDL is used to report alarms and performance data. The report is done by passing data or information outside the communication signal. Hence, the performance monitoring data or the maintenance information is gathered and passed along without interfering with the normal operation of the T1 line. The Performance Report Message (PRM) section in this application note defines the PRM as per the ANSI T1.403 standard and explains about mapping HDLC controllers to FDL to transmit and receive PRM using the registers of the DS2155. The Configuration of the HDLC Controllers section in this application note provides the configuration flowcharts for the HDLC engines for the transmit and receive paths.

The HDLC engine configuration described in this application note is specific to DS2155, but it can also be used to configure and initialize the HDLC engines of other devices such as the DS26514, DS26518, DS26521, DS26522, and DS26528 by mapping the registers of the DS2155 to that of these devices.

Acronym	Description
CRC	Cyclic Redundancy Check
ESF	Extended Super Frame
FDL	Facilities Data Link
HDLC	High-Level Data Link Control
PRM	Performance Report Message

Performance Report Message (PRM)

The ANSI T1.403 format offers the transmission of a PRM that permits the actual performance to be compared with established thresholds and generate an alert if abnormal conditions are detected. ANSI T1.403 uses a 4kbps channel called FDL provided by the Extended Super Frame (ESF) framing format.

Table 1. Example of Performance Report Messages for DS1 Data Link

	$i = i_o$	$i = i_o + 1$	$i = i_o + 2$	$i = i_o + 3$
Flag	01111110	01111110	01111110	01111110
Address Octet 1	00111000	00111000	00111000	00111000
Address Octet 2	00000001	00000001	00000001	00000001
Control	00000011	00000011	00000011	00000011
Message Octet 1	00000001	00000000	10000000	00100000
Message Octet 2	00000000	00000001	00000010	00000011
Message Octet 3	00000000	00000001	00000000	10000000
Message Octet 4	00010011	00000000	00000001	00000010
Message Octet 5	00000000	00000000	00000001	00000000
Message Octet 6	01000010	00010011	00000000	00000001
Message Octet 7	00000010	00000000	00000000	00000001
Message Octet 8	00000001	01000010	00010011	00000000
FCS Octet 1	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx
FCS Octet 2	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx

NOTES:
i = i_o - 3, slip = 1, all other parameters = 0, N(t) = 1
i = i_o - 2, severely-errored framing event = 1, all other parameters = 0, N(t) = 2
i = i_o - 1, CRC error events = 1, all other parameters = 0, N(t) = 3
i = i_o, CRC error events = 320, all other parameters = 0, N(t) = 0
i = i_o + 1, CRC error events = 0, all other parameters = 0, N(t) = 1
i = i_o + 2, CRC error events = 6, all other parameters =0, N(t) = 2
i = i_o + 3, CRC error events = 40, all other parameters =0, N(t) = 3

The receive HDLC controllers can be mapped to FDL by setting bit 6 of the HxRC register to 1.

Register Name H1RC, H2RC
Register Description HDLC #1 Receive Control
HDLC #2 Receive Control
Register Address 31h, 32h

Bit #	7	6	5	4	3	2	1	0
Name	RHR	RHMS	—	—	—	—	—	RFSD
Default	0	0	0	0	0	0	0	0

Bit 0/Receive SS7 Fill -In Signal Unit Delete (RFSD)
0 = normal operation; all FISU's are stored in the receive FIFO and reported to the host
1 = When a consecutive FISU having the same BSN the previous FISU is detected, it is deleted without host intervention

Bits 1 to 5/Unused, must be set to 0 for proper operation

Bit 6/Receive HDLC Mapping Select (RHMS)
0 = receive HDLC assigned to channels
1 = receive HDLC assigned to FDL (T1 mode), Sa bits (E1 mode)

Bit 7/Receive HDLC Reset RHR). Resets the receive HDLC controller and flushes the receive FIFO. Must be cleared and set again for subsequent reset.
0 = normal Operation
1 = reset the receive HDLC controller and flush the receive FIFO

The transmit HDLC controllers can be mapped to FDL by setting bit 4 of HxTC register to 1.

Register Name: **H1TC, H2TC**

Register Description: **HDLC #1 Transmit Control**
HDLC #2 Transmit Control

Register Address: **90h, A0h**

Bit #	7	6	5	4	3	2	1	0
Name	NOFS	TEOML	THR	THMS	TFS	TEOM	TZSD	TCRCD
Default	0	0	0	0	0	0	0	0

Bit 0/Transmit CRC Defeat (TCRDC). A 2 byte CRC code is automatically apppened to the outbound message. This bit can be used to disable the CRC function
0 = enable CRC generation (normal operation)

Bit 4/Transmit HDLC Mapping Select (THMS)
0 = transmit HDLC assigned to channels
1 = receive HDLC assigned to FDL (T1 mode), Sa bits (E1 mode)

Configuration of the HDLC Controllers

This device has two enhanced HDLC controllers: HDLC #1 and HDLC #2. Each controller can be configured to use with time slots, Sa4 to Sa8 bits (E1 mode), or the FDL (T1 mode). Each HDLC controller has 128-byte buffers in the transmit and receive paths. The user can select any time slot or multiple time slots besides specific bits within the time slot to assign to the HDLC controllers when used with time slots.

The HDLC controller performs the entire necessary overhead for generating and receiving PRMs as described in ANSI T1.403 and the messages as described in AT&T TR54016. The HDLC controller can automatically generate and detect flags, calculate the CRC checksum, and abort sequences. It can also automatically stuff and destuff zeros and align bytes to the datastream. The 128-byte buffers in the HDLC controller are large enough to allow a full PRM to be received or transmitted without host intervention.

The user must not map both transmit HDLC controllers to the same Sa bits, time slots or, in T1 mode, map both controllers to the FDL. HDLC #1 and HDLC #2 are identical in operation and therefore the following operational description refers only to a singular controller.

The HxTC and HxRC registers perform the basic configuration of the HDLC controllers. Operating features such as CRC generation, zero stuffer, transmit and receive HDLC mapping options, and idle flags are selected here. These registers also reset the HDLC controllers. When receiving or transmitting HDLC messages, the user can choose it to be interrupt driven, or the user can poll the desired status registers or a combination of these can also be used. See the following flowcharts for example routines for using the HDLC receiver (**Figure 1**) and HDLC transceiver (**Figure 2**).

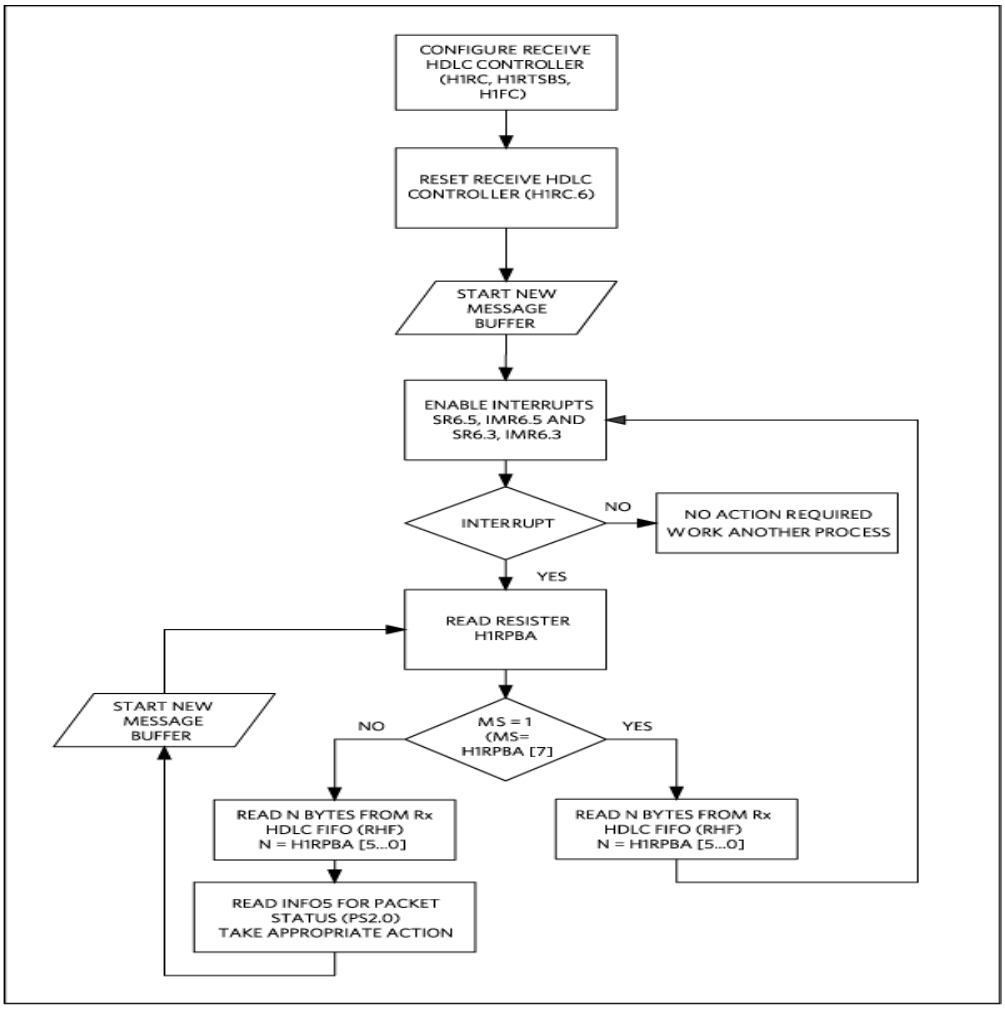

Figure 1. Receive HDLC configuration flowchart.

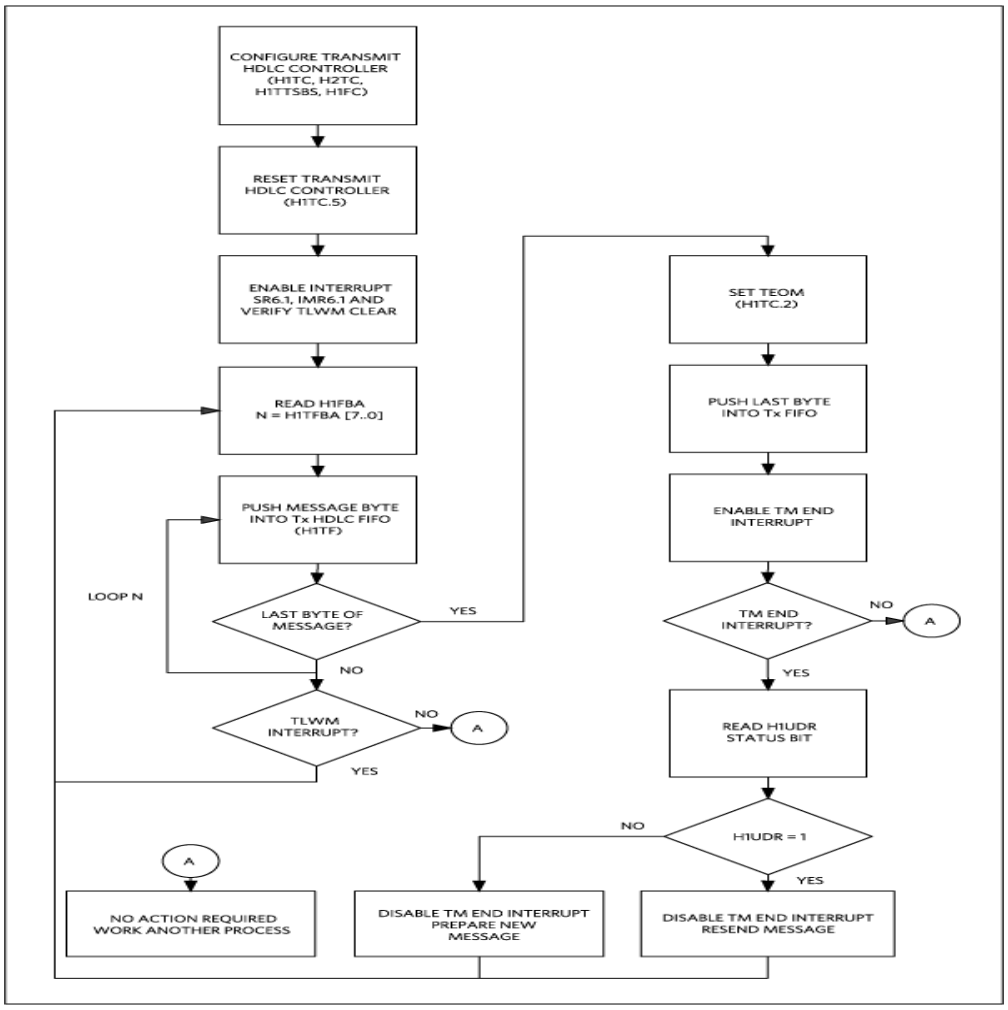

Figure 2. Transmit HDLC configuration flowchart.

Related Parts		
DS2155	T1/E1/J1 Single-Chip Transceiver	Free Samples
DS26514	4-Port T1/E1/J1 Transceiver	Free Samples
DS26518	8-Port T1/E1/J1 Transceiver	Free Samples
DS26521	Single T1/E1/J1 Transceiver	Free Samples
DS26522	Dual T1/E1/J1 Transceiver	Free Samples
DS26528	Octal T1/E1/J1 Transceiver	Free Samples

More Information
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